Instruction Manual

Tektronix

TMS809 AGP 3.0 Bus Support

071-1084-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Connect the ground lead of the probe to earth ground only.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate Without a Fan. Before operating this product, direct a fan at the probe head for proper cooling.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS809 AGP 3.0 Bus support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer, you only need this instruction manual to set up and run the TMS809 support package.

If you are not familiar with operating bus support packages, you need to supplement this instruction manual with information on basic operations of the logic analyzer to set up and run the TMS809 support package. See *Manual Conventions* below for more information.

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that decodes bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to your logic analyzer online help or logic analyzer user manual covering the basic operations of a bus support.
- The phrase “probe adapter” refers to the TMS809 support package software and hardware.
- The phrase “Front End board” refers to the circuit board that is used with both probe heads.

Contacting Tektronix

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Address	Tektronix, Inc. 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
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Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. - 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains a description of the probe adapter, and how to connect the logic analyzer to the target system.

Probe Adapter Description

The probe adapter allows the logic analyzer to acquire data from an Accelerated Graphics Port (AGP) bus (version 3.0) within the operating environment in the target system.

The probe adapter connects to the target system using the AGP 3.0 card connector. Signals from the bus flow from the probe adapter to the P6434 probes and through the probe cables to the logic analyzer.

The probe adapter package provides two probe heads:

- Interposer probe head (recommended for ease of use)
- Backside probe head (to use for lower target-system loading, if needed)

***NOTE**. When debugging an AGP Pro 1.5 V compatible graphic card, we recommend that you use the backside probe adapter.*

The probe adapter support package installs software that displays timing and state information from systems based on the AGP 3.0 bus. The software supports two AGP 3.0 modes of operation, AGP8X and AGP4X, along with the *PCI Local Bus Specification* (PCI) operations.

To use this probe adapter package efficiently, you may also refer to *Draft AGP V3.0 Interface Specification, Revision 0.95R, original date: May 2001 document* (Intel web site).

Logic Analyzer Software Compatibility

The label on the floppy disk states which version of logic analyzer software the probe adapter package is compatible with.

Logic Analyzer Configuration

To use the probe adapter you need a logic analyzer equipped with the minimum module configuration of three 136-channel, 100 MHz modules. For timing you need one 102 channel, 100 MHz module.

You can take state and asynchronous timing acquisitions simultaneously if four modules and 15 probes are available.

The probe adapter requires a minimum of twelve Mass Termination Probes.

You can connect probes as desired based on the following configurations:

- 12 mictor connectors for disassembly
- 3 mictor connectors for timing only

Labeling Probes

The probe adapter relies on the default channel mapping and labeling scheme for the probes. Apply labels using the instructions described in the following manuals. These manuals can be accessed from the Tektronix.com web site or these topics can be located in the logic analyzer online help:

- *P6434 Mass Termination Probe Instructions*
- *P6860 High Density Logic Analyzer Probe Label Instructions*

P6860 Probes

You can use the TLA7AXX 120 MHz logic analyzer module and the P6860 probes with the Compression-on-PCB to P6860 Mictor adapter to connect to the AGP 3.0 probe adapter package.

Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction manual*, 071-1059-XX, for more information. This manual can be accessed from the Tektronix.com web site or these topics can be located in the logic analyzer online help.

***NOTE**. When using the TLA7Axx modules with the TMS809 probe adapter, the analog outputs display the outputs of the digital buffers of the TMS809 and do not directly reflect the analog attributes of the AGP bus.*

Module Configuration

You must configure and merge the modules as shown in Figure 1–1. The memory depth is automatically chosen based on the shallowest memory depth of the merged modules.

The term “master module” refers to the middle module of a 3-wide merge. The term “slave module” refers to the module in the higher numbered slot than the master module. The term “slave 2” module refers to the module in the lower numbered slot than the master module.

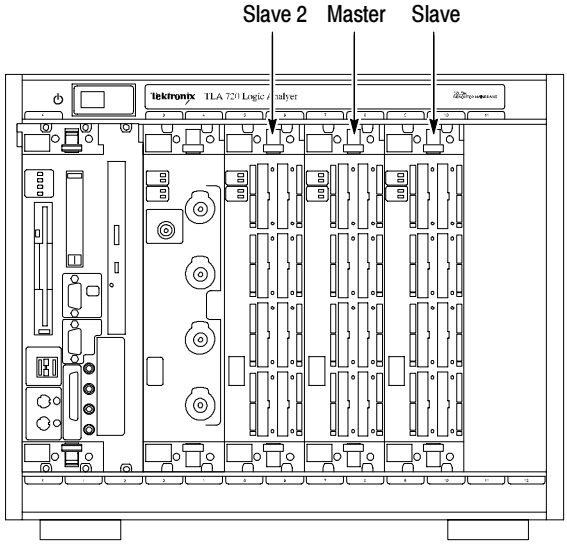

Figure 1- 1: Configuration of the slave 2, master, and slave modules

Acquisition Setup

The probe adapter software affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding bus-specific fields.

The probe adapter software adds the following selections to the Load Support dialog box, located under the File pulldown menu:

- AGP3_8X Disassembly mode
- AGP3_4X Disassembly mode
- AGP3_T Timing mode

After you load the software, the Custom Clocking mode selection in the module Setup menu is also enabled (see *Custom Clocking Mode* on page 2–3).

To use the AGP4X mode, refer to *Configuring the Probe Adapte*r on page 1–6. The AGP 3.0 probe adapter is shipped configured for the AGP8X mode.

Probe Adapter Review

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section in this manual as they pertain to the target system, as well as the following descriptions of other AGP 3.0 probe adapter package requirements and restrictions.

Hardware Reset. If a hardware reset occurs in the AGP 3.0 system during an acquisition, the application may acquire invalid samples until voltage levels stabilize.

System Clock Rate. The probe adapter can acquire data from the bus operating at speeds of up to 66 MHz. The AGP 3.0 probe adapter has been tested to a maximum Clock Rate of 66.625 MHz.

Functionality Not Supported

Review the functionalities that are not supported by the probe adapter package in the following descriptions:

Acquisition Channels. Extra acquisition channels are not available, since this probe adapter uses P6434 mictor connectors.

Sticky Address Bits. Sticky address bits are not tracked, stored, or displayed in TMS809 software package.

AGP 2.0 Bus. Although the probe adapter supports the AGP4X mode of operation on an AGP3.0 bus, the probe adapter does not support AGP4X on the AGP2.0 bus.

Dynamic Switching. Dynamic switching modes between AGP8X and AGP4X modes are not supported. To set up the AGP4X mode, refer to *Configuring the Probe Adapter* on page 1–6. The probe adapter is shipped from the factory in the AGP8X mode configuration.

Nonintrusive Acquisition. The probe adapter will not present signals back to the target system.

Components and Standard Accessories

The probe adapter is shipped with the following components and standard accessories:

- Probe adapter: Preprocessor unit, cables, Interposer probe head (attached), and Backside probe head
- Hardware
  - Positioning block and mounting plate with adhesive strips (one-time use and curing advised — see page 1–12)
  - Screws and washers (2 ea)
  - Extension nuts (4)
- AC power cord
- Document and software package: Includes the probe adapter manual, license agreement envelope with software disc, registration card, and statement of compliance envelope

For optional accessories, see the *Replaceable Parts List* on page 6–8.

Configuring the Probe Adapter

The probe adapter is configured for the AGP8X mode from the factory. To use either the AGP8X or the AGP4X modes, follow these steps:

1. Change the mode switch on the front of the preprocessor unit to AGP4X mode or AGP8X mode (see Figure 1–2).
2. Power the probe adapter off and on.
3. Reset the target system while in the chosen mode.

***NOTE**. The AGP4X mode is available only for AGP3.0 target systems.*

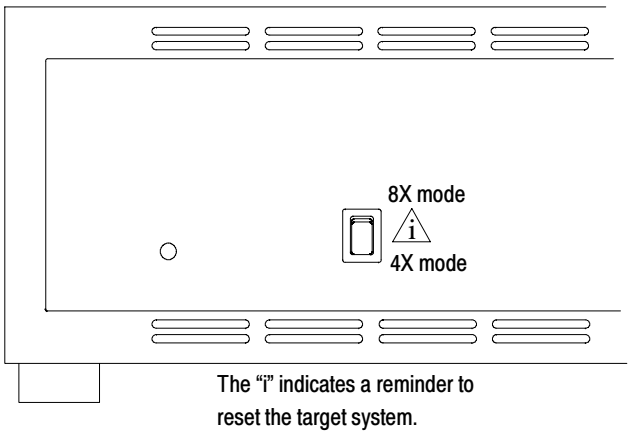

Figure 1-2: Switch for AGP8X or AGP4X mode

Connecting the Logic Analyzer to a Target System

We recommend that you use the Interposer probe head to connect the logic analyzer to the target system. If the target system functions improperly using the Interposer board, use the Backside probe head. If you use the Backside probe head, you need to remove the target system from the case that houses it.

***NOTE**. For storage and shipping, retain the cardboard cartons and packing material that is shipped with the probe adapter.*

***WARNING.** To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit. There are no operator serviceable parts inside the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

Tools Required. Following is a list of required tools:

- Nut driver (1/4 in) to remove the extension nuts from the Backside board assembly
- Phillips screwdriver (P2) to remove a probe head and to secure the Backside probe head
- Flat blade screwdriver to install the probe heads

Optional Tools. A torque wrench helps to ensure reliable connections by meeting the nominal torque values listed in these instructions.

See the following pages for these procedures:

- Interposer probe head installation (see page 1–8)
- Probe-head removal (see page 1–11)
- Backside probe head installation (see page 1–12)

***WARNING.** To prevent burns, forced air cooling is required across the probe adapter to maintain a temperature below 105 °C (220 °F). You must verify this temperature for the components and the probe adapter.*

CAUTION. *To prevent static damage to the power pod, probe adapter, probes, and module, handle components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the bus and probe adapter.

Connecting the Interposer Probe Head

For the first-time connection of the Interposer probe head to the AGP 3.0 signals in the target system, follow these steps:

NOTE*. If you are reconnecting the Interposer probe head, see* Reconnecting the Interposer Probe Head *on page 1-9.*

1. Power off the target system. It is not necessary to power off the logic analyzer.
2. Power off any probe adapters that may be attached to your target system. If the Backside probe head is attached, follow the instructions for *Removing a Probe Head* on page 1-11.
3. To discharge any stored static electricity, touch the ground connector located on the back of the logic analyzer.
4. Place the preprocessor unit on a horizontal, static free surface.

NOTE*. When debugging an AGP Pro 1.5 V compatible graphic card, we recommend that you use the backside probe adapter.*

5. Remove the AGP 3.0 bus card from the target system.
6. Connect the Interposer probe head to the target system as shown in Figure 1-3.
7. Connect the AGP 3.0 bus card to the Interposer probe head.

CAUTION. *To prevent damage to the probe adapter or target system when power is applied, connect the target system to the probe adapter properly.*

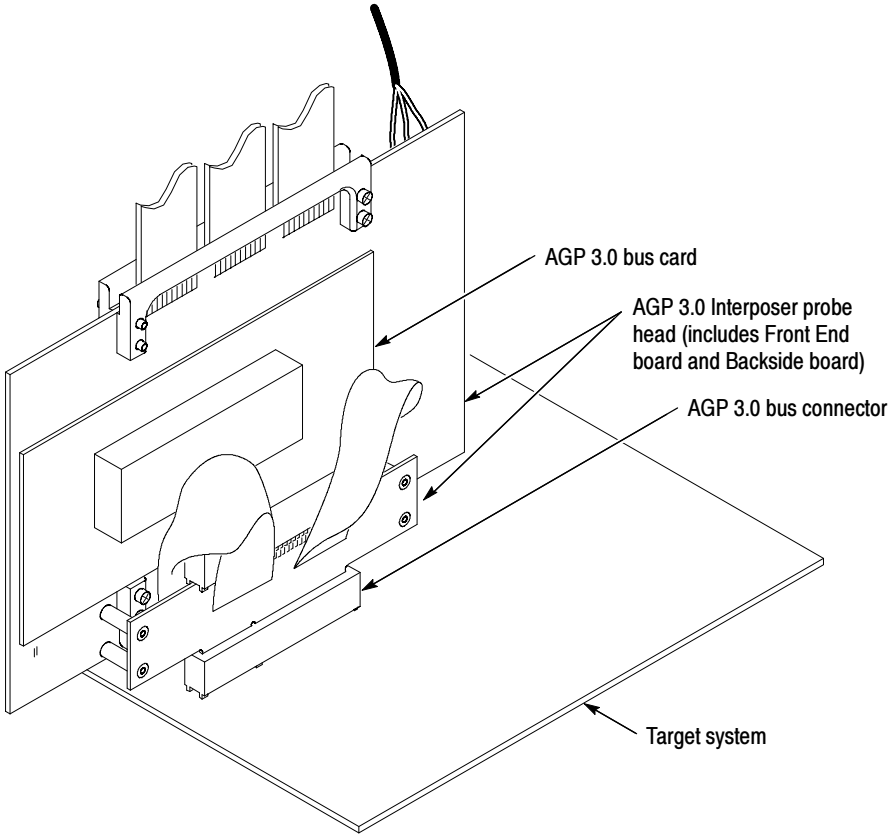

Figure 1-3: Connect the Interposer probe adapter to the AGP 3.0 bus connector

WARNING. *To prevent burns, forced air cooling is required across the probe adapter to maintain a temperature below 105 °C (220 °F). You must verify this temperature for the components and the probe adapter.*

8. Apply forced air cooling across the probe head.

Reconnecting the Interposer Probe Head

Before you begin to reconnect the Interposer probe head, check that no probe adapters are attached to the preprocessor unit and that the access panel on top of the preprocessor unit has been removed.

NOTE. *When debugging an AGP Pro 1.5 V compatible graphic card, we recommend that you use the backside probe adapter.*

1. Power off the preprocessor unit.
2. Power off the target system. You do not need to power off the logic analyzer.
3. Discharge the stored static electricity by touching the ground connector located on the back of the logic analyzer.

4. Connect the three small boards (attached to the probe-head cables), matching A to A, B to B, and C to C, to the Logic board. Access to the small board connections is through the access panel on top of the preprocessor unit (see Figure 1–4).

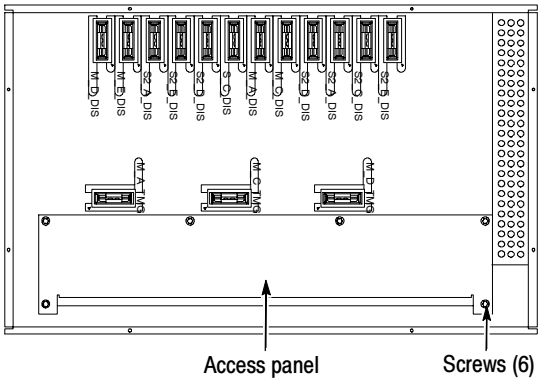

Figure 1-4: Preprocessor unit and access panel

5. Using a Phillips screwdriver, install the six screws into the three small boards (torque to 4 in-in/lb).

6. Using a Phillips screwdriver, attach the three power cables and the three screws (torque to 6 in/lb) to the Front End board (see Figure 1–5).

CAUTION. *To prevent damage to the probe adapter, check that the power cables are reattached to the Front End board correctly.*

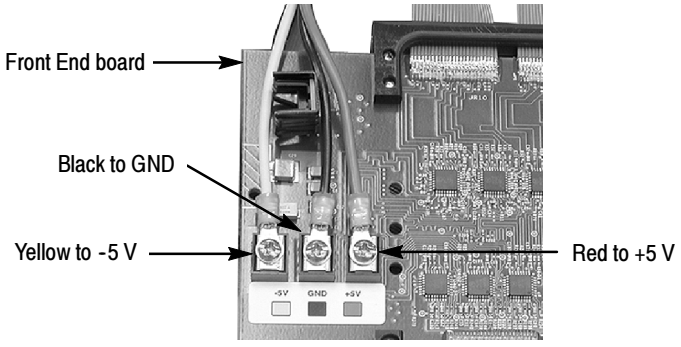

Figure 1-5: Attach the power cables

7. Hand start the screws that attach the access panel to the top of the preprocessor unit.

8. Using a Phillips screwdriver, tighten the screws (torque to 4 in/lb) in the access panel (see Figure 1–4).
9. Connect the Interposer probe head to the target system (go to step 6 on page 1–8 and complete the steps).

Removing a Probe Head

If you need to remove a probe head, follow these steps:

CAUTION. *To prevent static damage, handle these components only in a static-free environment. Static discharge can damage the probe adapter, the probes, and the logic analyzer module.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the probe adapter.

1. Power off the probe adapter and unplug the AC power cord on the preprocessor unit from the wall. The probe adapter power switch is located on the back of the preprocessor unit. It is not necessary to power off the logic analyzer.
2. Using a Phillips screwdriver, remove the screws from the access panel located on top of the preprocessor unit (see Figure 1–4). Set the access panel aside.
3. Using a Phillips screwdriver, remove the screws from the three small boards (attached to the probe-head cables). Access to the small boards is through the access panel on top of the preprocessor unit.
4. Disconnect the small boards from the Logic board.

NOTE*. Do not remove the power cables from the preprocessor unit.*

5. Remove the three screws and the three power cables from the Front End board. Set the screws aside for use later.

   Interposer probe head only — Disconnect the Interposer probe head from the target system. To properly store the Interposer probe head for use later, see *Storage* on page 1–26. To store the AGP 3.0 bus card, refer to the AGP 3.0 bus card information from the manufacturer. To reinstall the Interposer probe head, go to *Reconnecting the Interposer Probe Head* on page 1–9.

   Backside probe head only — To complete the removal procedure for the Backside probe head, follow these steps:

6. Using a Phillips screwdriver, remove the two screws from the center two holes on the Front End board assembly (see Figure 1–8 on page 1–17).

7. Remove the Front End board assembly from the Backside board assembly.
8. Using a nut driver, carefully remove the four extension nuts from the Backside board assembly (see Figure 1–7 on page 1–16).
9. Remove the Backside board from the mounting plate on the target system.

NOTE. *We recommend that you do not remove the mounting plate after it is attached to the target system.*

To properly store the Backside probe head for use later, see *Storage* on page 1–26.

Connecting the Backside Probe Head

To connect the Backside probe head to the signals on the target system, follow these steps:

1. Power off the target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle these components only in a static-free environment. Static discharge can damage the probe adapter, the probes, and the logic analyzer module.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the bus.

2. To discharge the stored static electricity, touch the ground connector located on the back of the logic analyzer.
3. Disconnect any attached probe adapters. See *Removing a Probe Head* on page 1–11.

NOTE. *Use an antistatic cushion to protect the components on the underside of the target system, because you will be applying pressure to the AGP 3.0 board.*

4. Place the target system on a horizontal, static-free surface (the back of the AGP 3.0 connector must be visible).

CAUTION. *To prevent replacing the mounting plate due to misalignment, place the mounting plate carefully on the back of the AGP 3.0 connector. You can use the mounting plate adhesive strips only once.*

After adhering the mounting plate to the target system, we recommend that you allow the adhesive strips to cure for 72 hours before attaching the Backside probe head to the target system. The adhesive strips are at 80% cure after 24 hours.

We recommend that you do not remove the mounting plate after it is attached to the target system.

5. Retrieve the mounting plate and the positioning block from the supplied standard accessories (see Figure 1–6).
6. Position the mounting plate near the top of the positioning block (see Figure 1–6).

7. Without removing the adhesive protector strips, test steps 9 and 10 to verify that obstructions do not exist and the mounting plate seats flush to the surface of the board. If there are obstructions, remove them.

CAUTION. *To prevent damage to the target system, the stud heads on the mounting plate must avoid target-system circuitry (see Figure 1–6). If they do not, use the Interposer probe head.*

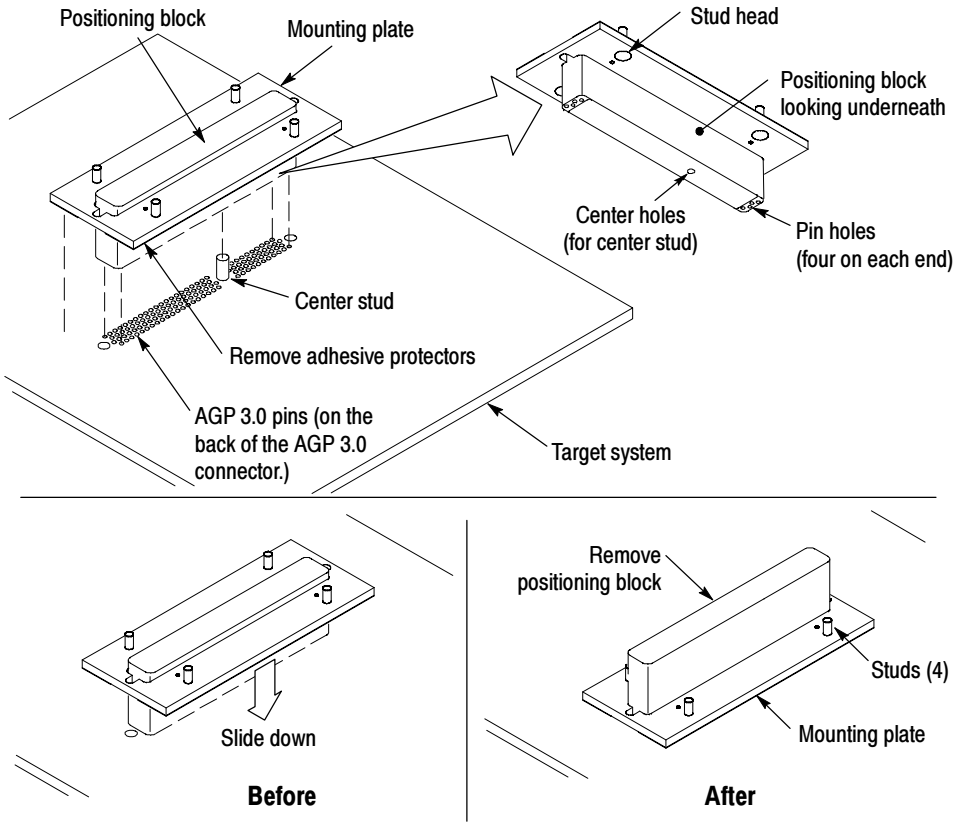

Figure 1-6: Attaching the mounting plate to the target system

8. Remove the adhesive protector strips from the mounting plate (see Figure 1–6).

9. Seat the positioning block on the back of the AGP 3.0 connector. Key the center stud to the hole on the bottom of the positioning block and align the eight pin holes on the positioning block to the pins on the AGP 3.0 connector (see Figure 1–6).

10. When you have seated the positioning block on the AGP 3.0 connector, slide the mounting plate into position. Securely adhere the mounting plate to the back of the AGP 3.0 connector by pressing evenly over the entire surface.

11. After the mounting plate is attached, remove the positioning block from the mounting plate. Discard the positioning block.

***NOTE**. For the first-time installation of the Backside probe head, you must remove the Front End board from the Backside board by removing the two screws and washers that attach the boards before continuing with the following steps (see Figure 1–8 on page 1–17).*

12. Key the four small holes on the Backside board assembly to the four mounting-plate studs. Guide the Backside board assembly into place on top of the mounting plate (see Figure 1–6 on page 1–14).

13. Insert the four extension nuts into the larger holes on the Backside board assembly (see Figure 1–7).

***CAUTION.** To avoid damage to the studs on the mounting plate, finger tighten the extension nuts (torque to 1 in/lb).*

14. Locate the four tab holes on the Front End board assembly (the side without the heatsink).

15. Insert the four tabs on the Backside board assembly into the four tab holes on the Front End board assembly, press into place.

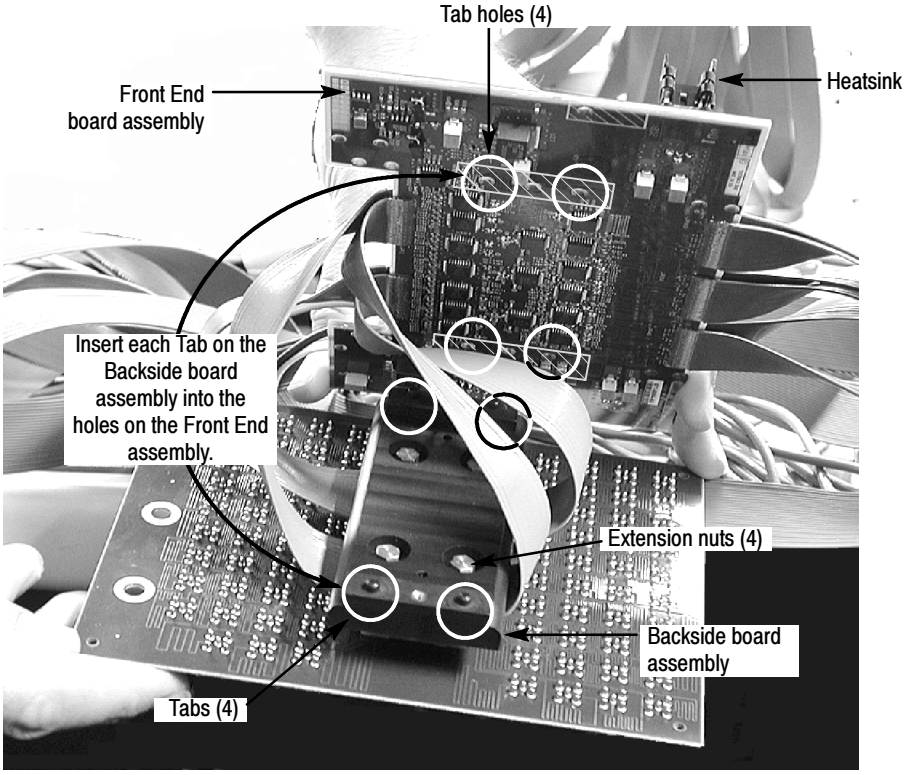

Figure 1-7: Attaching the Front End board assembly

***NOTE**. The two ribbon cables are captured between the two assemblies when the Backside probe head is properly installed.*

16. Align the center two holes on the Front End board to the holes on the Backside board. Heatsinks are visible when the Front End board is attached. Install two screws and two washer into the center two holes of the Front End board.

17. Using a flat-blade screwdriver, attach the Front End board assembly to the Backside board assembly, Torque to 5 in/lb (see Figure 1–8).

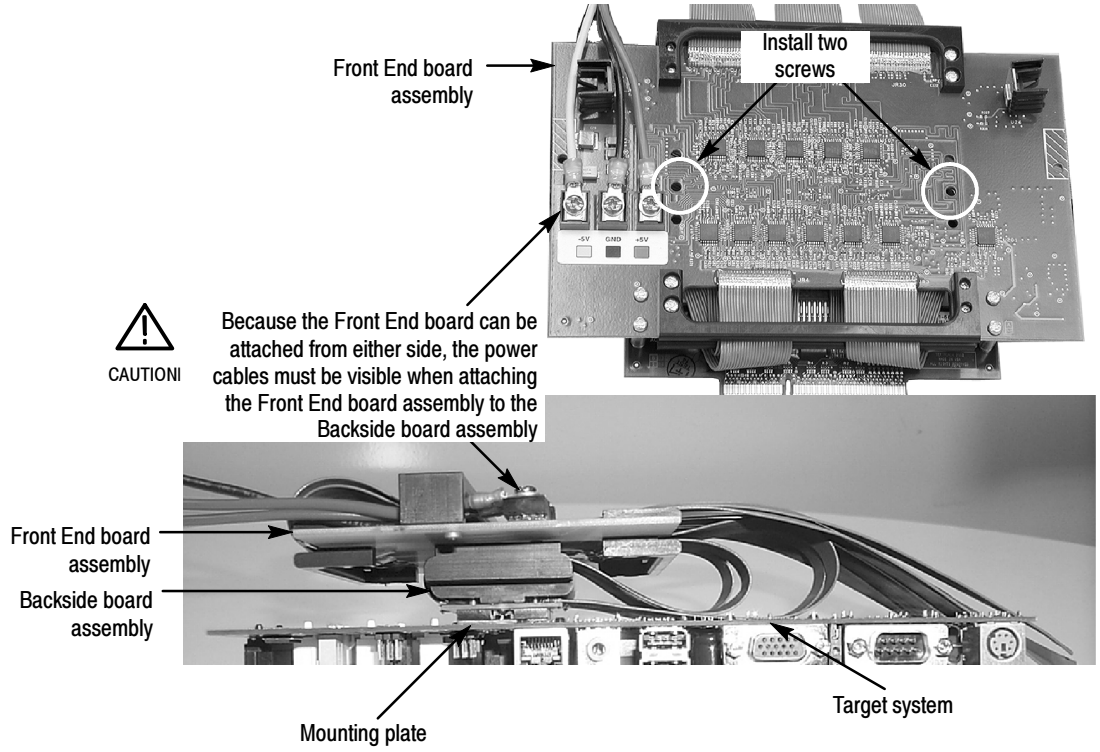

Figure 1-8: Assembled Backside probe head

18. Using a flat-blade screwdriver, install three screws and three power cables to the Front End board (see Figure 1–8).

CAUTION. *To prevent damage to the probe adapter, check that the three power cables are attached to the Front End board correctly (see Figure 1–9).*

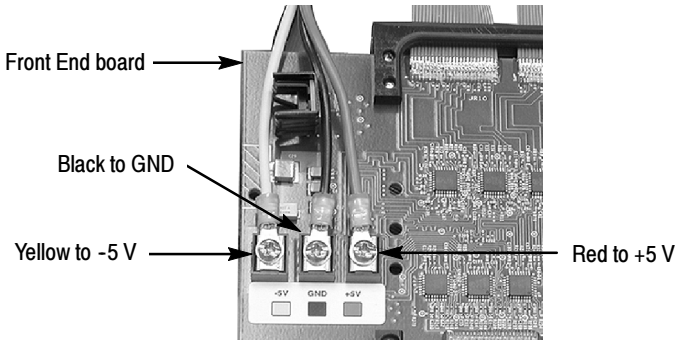

Figure 1-9: Attach the power cables

19. Connect the three small boards (attached to the probe-head cables), matching A to A, B to B, and C to C, to the Logic board. Access to the small boards is through the access panel on top of the preprocessor unit (see Figure 1–10).

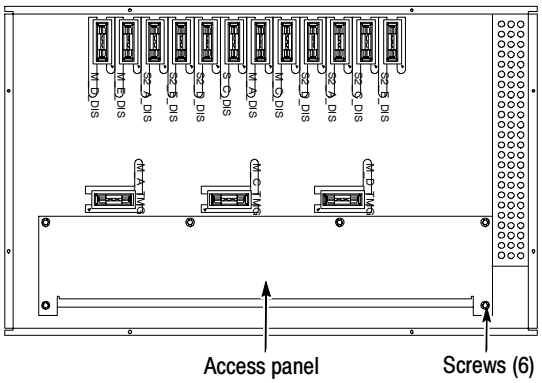

Figure 1-10: Preprocessor unit and access panel

20. Using a Phillips screwdriver, install six screws into the three small boards.

21. Position the access panel on top of the preprocessor unit and hand start the screws.

22. Using a Phillips screwdriver, tighten the screws in the access panel (torque to 4 in/lb).

WARNING. *To prevent burns, forced air cooling is required across the probe adapter to maintain a temperature below 105 °C (220 °F). You must verify this temperature for the components and the probe adapter.*

23. Apply forced air cooling across the probe head.

Connecting P6434 or P6860 Probes

Mictor connectors on the probe adapter may be configured for timing or disassembly software functions.

***NOTE**. For more detailed information about how to attach a P6860 probe or the mictor adapters, we recommend that you refer to the logic analyzer online help or the P6860 probe manual listed on page 1–2. Then proceed with connecting the probes for the minimum configuration for disassembly and timing software in this section.*

To view the P6860 probe and mictor adapters, see Figure 1–13 on page 1–22.

For reference, Figure 1–11 shows the module configuration for the Slave 2, Master, and Slave modules.

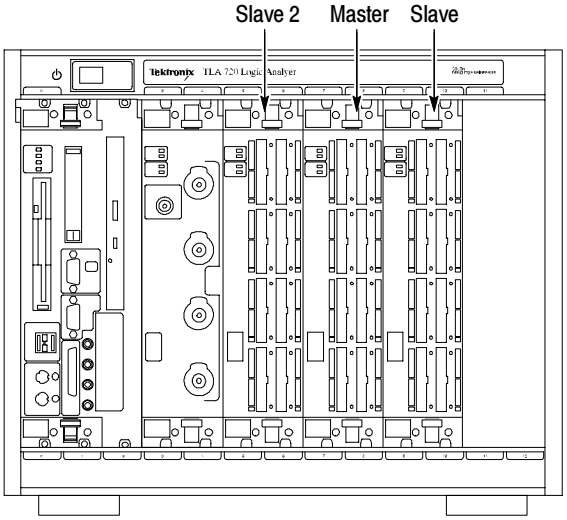

Figure 1- 11: Configuration of the slave 2, master, and slave modules

Disassembly. Following is the minimum probe configuration for disassembly software.

1. Match the A, D, C, and E probes from the Slave2 module with the corresponding S2_A_DIS, S2_D_DIS, S2_C_DIS, and S2_E_DIS probe connectors labels on the preprocessor unit. Align the pin 1 indicator on the probe label with the pin 1 indicator of the connector on the preprocessor unit.

CAUTION. *To prevent damage to the probe and preprocessor unit, always position the probe perpendicular to the mating connector with pin 1s aligned and then gently connect the probe. Incorrect handling of the probe while connecting to or disconnecting from the preprocessor unit can damage the probe or the mating connector on the preprocessor unit.*

2. Position the probe tip perpendicular to the mating connector, and gently connect the P6434 probe (see Figure 1–12). To attach a P6860 probe, skip steps 2 and 3 and refer to the probe manual listed on page 1–2.

3. When connected, push down on the latch releases on the probe to set the latch.

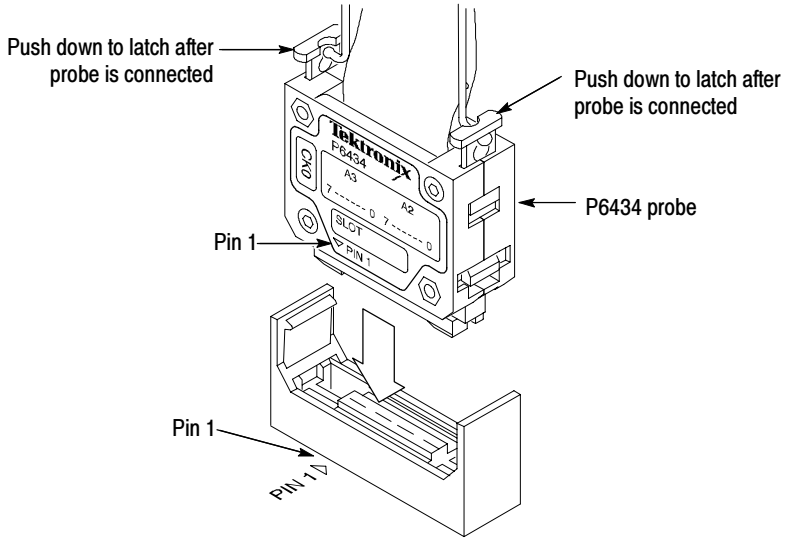

Figure 1- 12: Operating the P6434 probe latches

4. Match the A, D, C, and E probes from the Master module with the corresponding M_A_DIS, M_D_DIS, M_C_DIS, and M_E_DIS probe connectors labels on the preprocessor unit. Align the pin 1 indicator on the probe label with the pin 1 indicator of the connector on the preprocessor unit.

5. Repeat steps 2 and 3 to correctly connect the probes.

6. Match the A, D, C, and E probes from the Slave module with the corresponding S_A_DIS, S_D_DIS, S_C_DIS and S_E_DIS probe connector labels on the preprocessor unit. Align the pin 1 indicator on the probe label with pin 1 of the connector on the preprocessor unit (see Figure 1–12).

7. Repeat steps 2 and 3 to correctly connect the probes.

Timing. Following is the minimum probe configuration for timing software.

1. Match the A, D, and C probes from the Master module with the corresponding M_A_TMG, M_D_TMG, and M_C_TMG probe connectors labels on the preprocessor unit. Align the pin 1 indicator on the probe label with the pin 1 indicator of the connector on the preprocessor unit.

CAUTION. *To prevent damage to the probe and preprocessor unit, always position the probe perpendicular to the mating connector and then gently connect the probe. Incorrect handling of the probe while connecting to or disconnecting from the preprocessor unit can damage the probe or the mating connector on the preprocessor unit.*

2. Position the probe tip perpendicular to the mating connector, and gently connect the probe (see Figure 1–12). To attach a P6860 probe, skip steps 2 and 3 and refer to the probe manual listed on page 1–2.

3. When connected, push down on the latch releases on the probe to set the latch.

Figure 1–13 shows probes using mictor adapters with compression footprints. For more information about these probes, refer to page 1–2.

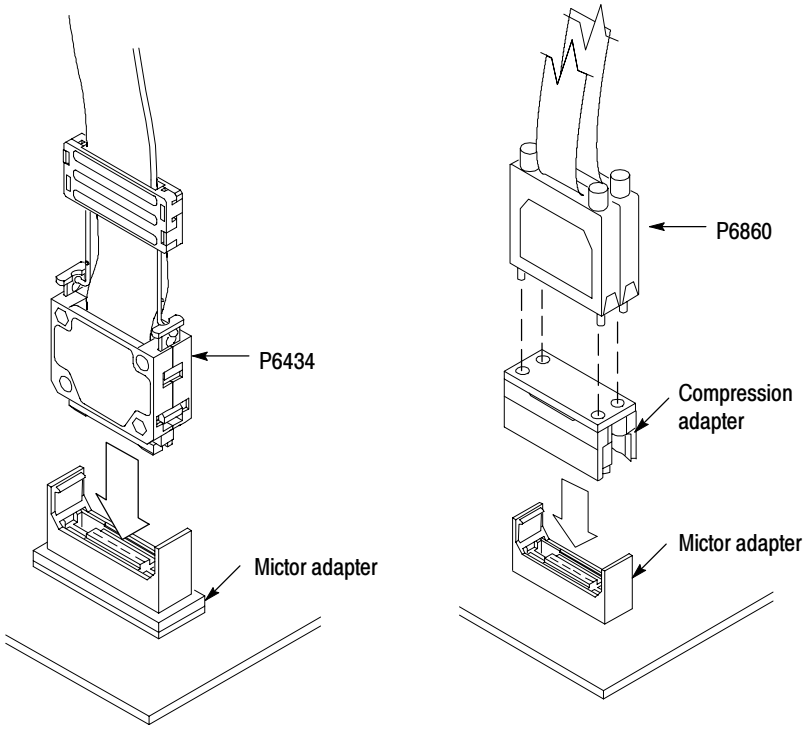

Figure 1-13: Probes with mictor adapters

Applying Power

To apply power to the AGP 3.0 probe adapter and target system, follow these steps:

WARNING. *To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit. There are no operator serviceable parts inside the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

1. Check that the power switch on the preprocessor unit is in the off position. If powered off, the zero (0) is visible on the power switch.
2. Plug the AC power cord into the IEC connector on the back of the preprocessor unit.
3. Plug the AC power cord into an electrical outlet that you know is working properly.
4. Power on the preprocessor unit. A green, power-on LED lights on the front of the preprocessor unit, indicating that the probe is active. If the LED does not light, see *Verifying Probe Operation* on page 1–23.
5. Power on the target system.

Removing Power

To remove power from the probe adapter, follow these steps:

1. It is not necessary to power off the target system or logic analyzer.
2. Power off the probe adapter at the back of the preprocessor unit.

Verifying Probe Operation

If you have trouble using the AGP 3.0 probe adapter to acquire data from the target system, use the following check list to ensure that the probe adapter and probe-head cables are working correctly.

WARNING. *To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit, except to verify probe head cable connections. There are no operator serviceable parts inside the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

1. Check that power is supplied to the preprocessor unit by observing the green LED on the front of the case. If the LED is not lighted:

- Check that the power switch on the back of the preprocessor unit is powered on. If powered off, a zero (0) is visible on the switch.
- Check that the AC power cord is plugged into an electrical outlet that you know is working properly.
- Check if the fans in preprocessor unit are rotating.
- Check the probe head cable connections through the opening in the top of the preprocessor unit (see Figure 1–14).
- If the LED is still not lighted, call a Tektronix application engineer.

2. Check that signals are passing through the mictor connectors by using the following procedure:

   a. Go to the setup menu and select “show activity”.

   b. Visually verify from the display that signals are transitioning on each mictor connector.

   c. If the signals are not transitioning, wiggle the mictor connector on top of the preprocessor unit slightly to check that it is fully seated.

   d. If the channels never transition:

   - Check the mictor probe for bent contacts.
   - Check the preprocessor unit for bent mictor contacts.

   If the preceding bulleted items did not correct the problem, replace the existing mictor probe with a new mictor probe.

   e. If the signals are still not transitioning, disconnect the mictor probe from that socket in the preprocessor unit. Then plug the mictor probe into a socket that is transitioning signals.

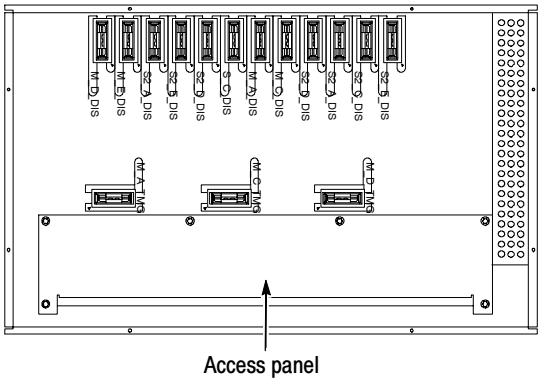

Figure 1-14: Preprocessor unit and access panel

Replacing the Pogo Pin Assembly (Backside Board)

To replace the Pogo pin assembly, follow these steps:

1. Power off the target system. It is not necessary to power off the logic analyzer.
2. Power off the probe adapter at the back of the preprocessor unit.
3. Disconnect the Backside probe head from the target system. Go to *Removing a Probe Head* on page 1–11. Start with step 1, then skip to step 6 and end at step 9.

CAUTION. *To prevent the Pogo pins from falling out of the assembly during removal, grasp the top and bottom of the assembly during removal. Before releasing the assembly, check that all four spiral pins are attached to the Pogo pin assembly. Reinstall any missing spiral pins.*

To prevent damage to the target system, position the Pogo pin assembly as shown in Figure 1–15.

4. After the Backside probe head is disconnected, remove the two screws from the Pogo pin assembly (see Figure 1–15). Remove the Pogo pin assembly.
5. Using the spiral pins on the Pogo pin assembly as keys, slide the new Pogo pin assembly onto the Backside board.
6. Using a Phillips screwdriver and two screws, align and attach the Pogo pin assembly (torque to 4 in/lb) to the Backside board.

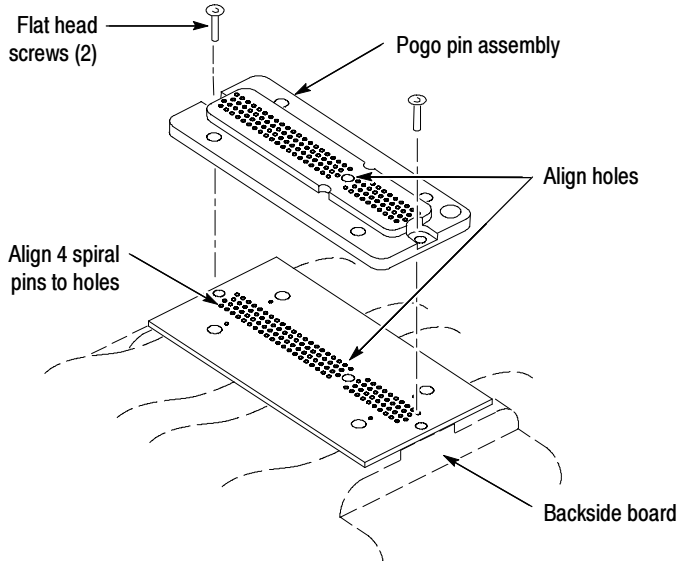

Figure 1-15: Replacing the Pogo pin assembly on the Backside board

Storage

The storage instructions describe short- and long-term storage of the probe head, cables, and preprocessor unit.

CAUTION. *To prevent damage to the sensitive probe-head cables, dress the cables to not pinch or contact any sharp objects. When you fold the cables use a minimum radius of 0.25 (0.64 cm) at the fold.*

Short-Term Storage

For short-term storage follow these steps:

1. Power off the probe adapter. You can leave the logic analyzer powered on.
2. Disconnect the probe head. See *Removing a Probe head* on page 1–11 for the Interposer probe head and for the Backside probe head.
3. Place the Interposer probe head in the black shipping carton and store with the preprocessor unit. If the shipping carton is not available, wrap pink antistatic bubble wrap around the probe head. Store the Backside probe head in an antistatic bag.

Long-Term Storage

For long-term storage; use the existing cardboard carton, black carton, and packaging, and follow these steps:

1. Power off the probe adapter. You can leave the logic analyzer powered on.
2. Disconnect the preprocessor unit from the logic analyzer by removing the P6434 probes from the top of the preprocessor unit.
3. Unplug the AC power cord from the IEC connector on the back of the preprocessor unit.
4. Disconnect the probe head. See *Removing the Probe head* on page 1–11 for the Interposer probe head and for the Backside probe head.
5. Place the preprocessor unit inside the antistatic bag.
6. Place the Interposer probe head in the black carton and fold the carton over the top of the preprocessor unit. Store the unused probe head in an antistatic bag.

CAUTION. *To prevent damage to the sensitive probe-head cables, dress the cables to not pinch or contact any sharp objects. When you fold the cables use a minimum radius of 0.25 (0.64 cm) at the fold.*

7. Place the foam end caps on both sides of the preprocessor unit. The depression on the foam end caps is positioned up.

8. Place the preprocessor unit inside the cardboard carton.
9. Place the cardboard accessory tray on top of the foam end caps. Close the carton.

Care and Maintenance

Before cleaning this product, read the following information:

CAUTION. *Static discharge can damage the probe adapter, the probes, and the module. To prevent static damage, handle components only in a static-free environment.*

The TMS809 AGP 3.0 probe adapter does not require scheduled or periodic maintenance. However, to maintain good electrical contact and efficient heat dissipation, keep the probe adapter free of dirt, dust, and contaminants. When not in use, store the probe adapter in the original shipping bags and cardboard cartons (see *Storage* on page 1–26)**.**

External Cleaning Only

Clean dirt and dust with a soft bristle brush. For more extensive cleaning, use only a damp cloth moistened with deionized water; do not use any other chemical cleaning agents.

WARNING. *To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit for cleaning. There are no operator serviceable parts inside the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

Shipping the Probe Adapter

To commercially transport the TMS809 AGP 3.0 probe adapter, package as follows:

1. Use the existing cardboard shipping cartons. If the existing shipping cartons are not available, use a double-walled, corrugated cardboard shipping carton with dimensions that are three inches (7.62 cm) larger on each side and top of the carton than the probe adapter.
2. If you are shipping the probe adapter to a Tektronix service center for Warranty service, attach a tag to the probe adapter showing the following:
   - Owner's name and address
   - Name of a person who can be contacted
   - Probe adapter type and serial number
   - Description of the problem
3. Place the preprocessor unit in the antistatic bag.
4. Place the probe head and cables in the black shipping carton, and fold the black shipping carton over the top of the preprocessor unit.

CAUTION. *To prevent damage to the sensitive probe-head cables, dress the cables to not pinch or contact any sharp objects. When you fold the cables use a minimum radius of 0.25 (0.64 cm)at the fold.*

5. Place the foam end caps on both sides of the preprocessor unit. The depression on the foam end caps are positioned up.

   If the foam end caps are not available, tightly pack dunnage or urethane foam between the cardboard carton and the probe adapter allowing 3 inches (7.62 cm) on each side to cushion the probe adapter.
6. Place the preprocessor unit inside the cardboard carton.
7. Place the cardboard accessory tray on top of the probe adapter. Close and tape the cardboard carton.
8. Ship the probe adapter.

Operating Basics

Setting Up the Software

This section provides information on how to set up the TMS809 AGP 3.0 Bus software on any Tektronix logic analyzer along with the following topics:

- Channel group definitions and symbol table overview
- Support package setups
- Disassembled Data

Basic information for general tasks and functions are described in the Tektronix logic analyzer online help or the Tektronix logic analyzer user manual.

Before you acquire and display disassembled data, you must load the support and specify setups for clocking as described in the information on basic operations. The support provides default values for the setups, but you can change them as needed.

Installing the Software

NOTE. *Before you install any software, we recommend that you verify the bus support software is compatible with the logic analyzer software.*

To install the TMS809 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Select the Windows Start button, point to Settings, and select Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You must close all windows before you uninstall any software.

Support Package Setups

The TMS809 AGP 3.0 software package installs three setup support files. Each setup provides different clocking and display options. All channels are displayed as active high.

AGP3_8X Setup This setup provides disassembly support for the AGP3_8X bus.

AGP3_4X Setup This setup provides disassembly support for the AGP3_4X bus.

NOTE. *To use the AGP4X mode see* Configuring the Probe Adapter *on page 1-6.*

AGP3_T Setup This setup provides timing support.

Channel Group Definitions

The TMS809 AGP 3.0 software package automatically defines channel groups for each installed support setup. The channel groups for the AGP 3.0 software support are SBA[7:0]#, Command, AD[31:0], C#_BE[3:0], Control, Status, and Misc. If you want to know which signal is in which channel group, refer to the channel assignment tables beginning on page 3-25.

For additional information on bus signals for the probe adapter, see page 3-43.

Symbol Tables

For channel groups with an associated symbol table file, you can set the display radix to Symbolic and select the proper symbol table by using the column properties dialog in the listing window display.

Symbol Tables begin on page 3-1. Following is a list of the symbol table file names:

AGP3_Command
AGP3_Status
AGP3_Control
AGP3_SBA_Cmd

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it dissembled. For additional information about channel tables see page 3–5.

Acquiring Data

After you load the AGP 3.0 bus support package and choose a clocking option, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations, logic analyzer online help, or Appendix A: *Error Messages and Disassembly Problems* in the logic analyzer user manual.

Clocking

The module acquires AGP 3.0 signals using the TMS809 AGP 3.0 bus support software and probe adapter.

For correct disassembly, do not use the Internal or External clocking modes. The logic analyzer online help describes in more detail how to use these clock selections for general purpose analysis.

- Internal clocking (used for timing) is based on the clock generated by a Tektronix logic analyzer. You can configure the clock rate from 50 ms down to 4 ns. For the TLA7XX, you can configure the clock rate to 2 ns.
- External clocking is used when you configure the clocking of data based on logical combinations of clocks and qualifiers.

Custom Clocking Mode

A special clocking program is loaded to the module every time you load the AGP 3.0 bus support package. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the AGP 3.0 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

Custom Clocking Menu Options. The only custom clocking option available is Clock-by-Clock.

Clock-by-Clock. This custom clocking option acquires all channels on every rising edge of the AGP CLK signal, except during reset, where only one sample is acquired. Invalid phases are represented as dashes.

Active Cycles Only. Active Cycles Only mode clocks in only those cycles which have valid data on the AD[31:0], SBA[7:0], C/BE[3:0]#, and the ST[2–0] buses.

This clocking mode is enabled only after you set up menu definitions in the Storage definition window (see Figure 2–1). Use the following procedure:

1. Load the support package.
2. From the system window, select the logic analyzer Trigger 

button.
3. Select the Power Trigger tab.
4. In the Storage menu, select Conditional.
5. From the Storage Definition window, select the If button and either Channel or Group from the menu.
6. For each row in the Storage Definition window, select the menu definition shown in Figure 2–1.

***NOTE**. When AGP4X mode is enabled the same menu definitions are selected, except channel **4X**/PCI#_AD and omit groups 4–SBA[7:0]# and 6_SBA[7:0]#.*

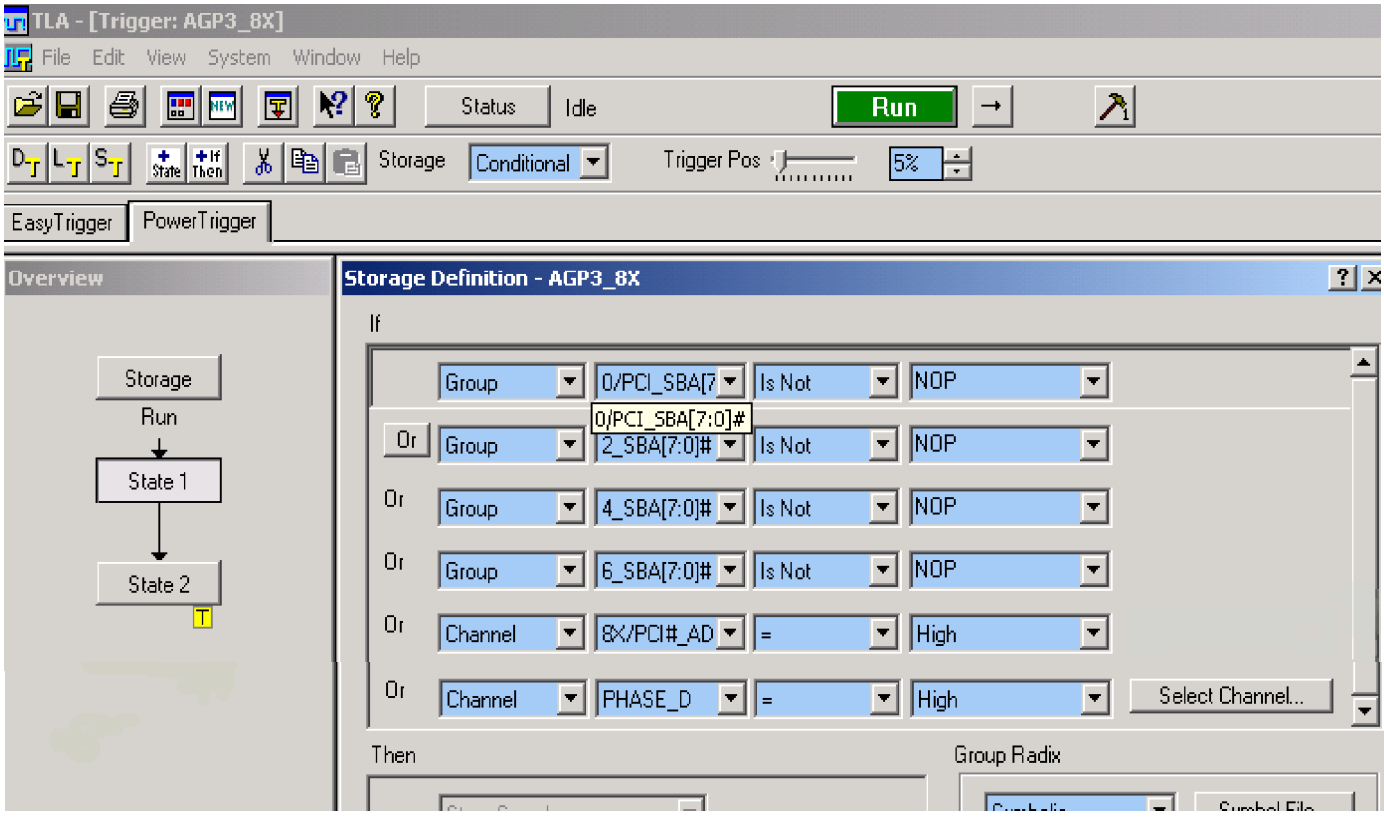

Figure 2–1: Select these definitions for AGP8X

Viewing Disassembled Data

You can view acquired data in two formats: Listing and Waveform. The information on basic operations describes how to select the disassembly display formats.

Table 2–1 shows the waveforms that are displayed when using the AGP 3.0 support package.

Table 2-1: Waveform displays

AGP 3.0 support signal name	AGP 3.0 disassembly support	AGP3_T support
CLK	X	X
AD_STBF0	-	X
AD_STBS0	-	X
AD[15-0]	-	X
AD_STBF1	-	X
AD_STBS1	-	X
AD[31-16]	-	X
[0-7]_AD[31-0]	X	-
Command	X	-
SBA[7:0]	-	X
[0-7]_SBA[7:0]	X	-
SBA_STBF	-	X
SBA_STBS	-	X
C#_BE[3:0]	-	X
[0-7]_C#_BE[3:0]	X	-
ST2	X	X
ST1	X	X
ST0	X	X
FRAME#	X	X
IRDY#	X	X
TRDY#	X	X
RBF#	X	X
WBF#	X	X
STOP#	X	X
DEVSEL#	X	X
REQ#	X	X

Table 2-1: Waveform displays (Cont.)

AGP 3.0 support signal name	AGP 3.0 disassembly support	AGP3_T support
GNT	X	X
RESET#[1]	X	X

1 # Indicates that the signal is asserted low

Table 2–2 lists the default display radix for the AGP 3.0 channel groups.

Table 2-2: Default display radix

Group name	State default display radix	Disassembly default display radix
0/ SBA[7:0]#	BIN	OFF
1_SBA[7:0]#	BIN	OFF
2_SBA[7:0]#	BIN	OFF
3_SBA[7:0]#	BIN	OFF
4_SBA[7:0]# ‡	BIN	OFF
5_SBA[7:0]# ‡	BIN	OFF
6_SBA[7:0]# ‡	BIN	OFF
7_SBA[7:0]# ‡	BIN	OFF
SBA	D/O†	SYM
Mnemonics	D/O†	TEXT
0/PCI_AD[31:0]	HEX	OFF
1_AD[31:0]	HEX	OFF
2_AD[31:0]	HEX	OFF
3_AD[31:0]	HEX	OFF
4_AD[31:0] ‡	HEX	OFF
5_AD[31:0] ‡	HEX	OFF
6_AD[31:0] ‡	HEX	OFF
7_AD[31:0] ‡	HEX	OFF
Addr/Data	D/O†	HEX
0/PCI_C#_BE[3:0]	HEX	OFF
1_C#_BE[3:0]	HEX	OFF
2_C#_BE[3:0]	HEX	OFF
3_C#_BE[3:0]	HEX	OFF
4_C#_BE[3:0] ‡	HEX	OFF
5_C#_BE[3:0] ‡	HEX	OFF
6_C#_BE[3:0] ‡	HEX	OFF
7_C#_BE[3:0] ‡	HEX	OFF

Table 2-2: Default display radix (Cont.)

Group name	State default display radix	Disassembly default display radix
PCI Cmd	D/O†	TEXT
Control	SYM	OFF
Command	SYM	OFF
Status	SYM	OFF
Misc	HEX	OFF

† **D/O: Disassembly only**

‡ **Signal omitted on 4X support**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your software support disc. This example shows you how the bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to the target system.

Reference

Symbol Tables

This section contains symbol tables Tables 3–1 through 3–4.

Table 3–1 lists the name, bit pattern, and meaning for the symbols in the file AGP3_Command, the Command channel group symbol table.

Table 3-1: AGP3_Command symbol table definitions

	Command group value			
Symbol	IRDY	FRAME FRAME_L 8X/PCI#_AD_D	C#BE3 C#BE2 C#BE1 C#BE0	Description
PCI_Int_Ack	0	100	1111	PCI Interrupt Acknowledge
PCI_Special	0	100	1110	PCI Special Command
PCI_I/O_Rd	0	100	1101	PCI Input/Output Read
PCI_I/O_Wr	0	100	1100	PCI Input/Output Write
PCI_Mem_Rd	0	100	1001	PCI Memory Read
PCI_Mem_Wr	0	100	1000	PCI Memory Write
PCI_Config_Rd	0	100	0101	PCI Configuration Read
PCI_Config_Wr	0	100	0100	PCI Configuration Write
PCI_Mem_Rd_Mul	0	100	0011	PCI Memory Read Multiple
PCI_Ext_Addr	0	100	0010	PCI Extended Address
PCI_Mem_Rd_Line	0	100	0001	PCI Memory Read Line
PCI_Mem_Rd_Inv	0	100	0000	PCI Memory Write and Invalidate
PCI_I/O_R/W	0	100	110X	PCI Input/Output Read/Write
PCI_Mem_R/W	0	100	100X	PCI Memory Read/Write
PCI_Config_R/W	0	100	010X	PCI Configuration Read/Write
PCI_Cmd	0	100	XXXX	Any PCI Command
~	1	100	XXXX	PCI data
-	1	XXX	XXXX	Reserved/Undefined

Table 3–2 lists the name, bit pattern, and meaning for the symbols in the file AGP3_Status, the Status channel group symbol table.

Table 3-2: AGP3_Status symbol table definitions

Symbol	Status group value ST2 ST1 GNT# ST0	Description
-	1 XXX	Grant Not Asserted
Grant	1 111	Transaction Request
Read	1 000	Read Transaction
Write	1 010	Write Transaction
Calibrate	1 110	Calibration Cycle
Rd/Wr	1 0X0	Read or Write Transaction
Reserved	1 XXX	Reserved Status Code

Table 3–3 lists the name, bit pattern, and meaning for the symbols in the file AGP3_Control, the Control channel group symbol table.

Table 3-3: AGP3_Control symbol table definitions

Symbol	Control group value RST# RBF REQ IRDY PME# SERR GNT TRDY PERR FRAME DEVSEL PAR FRAME_L STOP 8X/PCI#_AD_D	Description
Reset	0X XXXX XXXXX XXXX	Reset
Sys_Err	1X X1XX XXXXX XXXX	System Error
Par_Err	1X XX1X XXXXX XXXX	Parity Error
PCI_Cmd	1X XXXX XX100 XXXX	PCI Address
PCI_Data	1X XXXX XXX10 XXXX	PCI Data
PCI_Abort	1X XXXX XXXX0 1X01	PCI Target Abort
PCI_Discon	1X XXXX XXXX0 1X11	PCI Target Disconnect
IRDY_TRDY	1X XXXX XXXXX 11XX	IRDY/TRDY Asserted
IRDY	1X XXXX XXXXX 1XXX	IRDY Asserted
TRDY	1X XXXX XXXXX X1XX	TRDY Asserted
Rd_Buf_Fl	1X 1XXX XXXXX XXXX	Read Buffer Full
Grant	1X XXXX X1XXX XXXX	Grant Asserted
Request	1X XXXX 1XXXX XXXX	Request Asserted

Table 3-3: AGP3_Control symbol table definitions (Cont.)

Symbol	Control group value				Description
	RST# / PME#	RBF / SERR / PERR / PAR	REQ / GNT / FRAME / FRAME_L / 8X/PCI#_AD_D	IRDY / TRDY / DEVSEL / STOP	
Stop	1X	XXXX	XXXXX	XXX1	Stop Asserted
Dev_Sel	1X	XXXX	XXXXX	XX1X	Device Select Asserted
Frame	1X	XXXX	XX1XX	XXXX	Frame Asserted
Pwr_Mgmt_Ev	10	XXXX	XXXXX	XXXX	Power Management Event
PAR	1X	XXX1	XXXXX	XXXX	Pipe Asserted
-	11	000X	000XX	0000	Bus inactive

Table 3-4 lists the name, bit pattern, and meaning for the symbols in the file AGP3_SBA_Cmd, the SBA_Cmd channel group symbol table.

Table 3-4: AGP3_SBA_Cmd symbol table definitions

Symbol	SBA_Cmd group value SBA7# SBA6# SBA5# SBA4# SBA3# SBA2# SBA1# SBA0#	Description
SYNC	1111 1110	synchronization cycle
NOP	1111 1111	NOP
Type_4	1110 XXXX	Extended address
Type_3	1100 XXXX	Upper address
Invalid	1101 XXXX	Type 3, invalid reserved bit
Rd_Async	1000 000X	Asynchronous Read (formerly Rd_LP)
Reserved	1000 010X	(formerly Rd_HP)
Reserved	1000 100X	---
Rd_ISOCH	1000 110X	Isochronous Read Command
Wr_Async	1001 000X	Asynchronous Write (formerly Wr_LP)
Reserved	1001 010X	(formerly Wr_HP)
Wr_ISOCH_Unfncd	1001 100X	Isochronous Write Unfenced (out-of-order completion)
Wr_ISOCH_Fenced	1001 110X	Isochronous Write Fenced (ordered completion)
Reserved	1010 000X	(formerly L_Rd_LP)
Reserved	1010 010X	(formerly L_Rd_HP)
Flush	1010 100X	Flush - Similar to Read
Reserved	1010 110X	---
Fence	1011 000X	Fence
Reserved	1011 010X	PCI - Dual Address Cycle
Align_ISOCH	1011 100X	Returns time offset of corelogic
Reserved	1011 110X	---
Invalid	10XX XX1X	Type 2, invalid reserved bit
Type_1	0XXX XXXX	Lower address and command
Reserved	1111 0XXX	Reserved command

Channel Group Definition Tables

This section contains Channel Group Definition Tables 3–5 through 3–13 for both the AGP3_8X and the AGP3_4X support packages with the following exceptions.

***NOTE**. The following tables with channel names that are prefixed with 4_, 5_, 6_, and 7_, are not used in the AGP3_4X support setup.*

Channel assignments shown in Tables 3–5 through 3–32 use the following conventions:

- A pound sign (#) following a signal name indicates an active low signal.
- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).

Table 3–5 lists the group definitions for the 7_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-5: 7_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	7_AD31
30	7_AD30
29	7_AD29
28	7_AD28
27	7_AD27
26	7_AD26
25	7_AD25
24	7_AD24
23	7_AD23
22	7_AD22
21	7_AD21
20	7_AD20
19	7_AD19
18	7_AD18

Table 3-5: 7_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
17	7_AD17
16	7_AD16
15	7_AD15
14	7_AD14
13	7_AD13
12	7_AD12
11	7_AD11
10	7_AD10
9	7_AD9
8	7_AD8
7	7_AD7
6	7_AD6
5	7_AD5
4	7_AD4
3	7_AD3
2	7_AD2
1	7_AD1
0	7_AD0

Table 3-6 lists the group definitions for the 6_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-6: 6_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	6_AD31
30	6_AD30
29	6_AD29
28	6_AD28
27	6_AD27
26	6_AD26
25	6_AD25

Table 3-6: 6_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
24	6_AD24
23	6_AD23
22	6_AD22
21	6_AD21
20	6_AD20
19	6_AD19
18	6_AD18
17	6_AD17
16	6_AD16
15	6_AD15
14	6_AD14
13	6_AD13
12	6_AD12
11	6_AD11
10	6_AD10
9	6_AD9
8	6_AD8
7	6_AD7
6	6_AD6
5	6_AD5
4	6_AD4
3	6_AD3
2	6_AD2
1	6_AD1
0	6_AD0

Table 3–7 lists the group definitions for the 5_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-7: 5_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	5_AD31
30	5_AD30
29	5_AD29
28	5_AD28
27	5_AD27
26	5_AD26
25	5_AD25
24	5_AD24
23	5_AD23
22	5_AD22
21	5_AD21
20	5_AD20
19	5_AD19
18	5_AD18
17	5_AD17
16	5_AD16
15	5_AD15
14	5_AD14
13	5_AD13
12	5_AD12
11	5_AD11
10	5_AD10
9	5_AD9
8	5_AD8
7	5_AD7
6	5_AD6
5	5_AD5
4	5_AD4
3	5_AD3

Table 3-7: 5_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
2	5_AD2
1	5_AD1
0	5_AD0

Table 3–8 lists the group definitions for the 4_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-8: 4_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	4_AD31
30	4_AD30
29	4_AD29
28	4_AD28
27	4_AD27
26	4_AD26
25	4_AD25
24	4_AD24
23	4_AD23
22	4_AD22
21	4_AD21
20	4_AD20
19	4_AD19
18	4_AD18
17	4_AD17
16	4_AD16
15	4_AD15
14	4_AD14
13	4_AD13
12	4_AD12
11	4_AD11
10	4_AD10

Table 3-8: 4_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
9	4_AD9
8	4_AD8
7	4_AD7
6	4_AD6
5	4_AD5
4	4_AD4
3	4_AD3
2	4_AD2
1	4_AD1
0	4_AD0

Table 3–9 lists the group definitions for the 3_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-9: 3_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	2_AD31
30	2_AD30
29	2_AD29
28	2_AD28
27	2_AD27
26	2_AD26
25	2_AD25
24	2_AD24
23	2_AD23
22	2_AD22
21	2_AD21
20	2_AD20
19	2_AD19
18	2_AD18
17	2_AD17

Table 3-9: 3_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
16	2_AD16
15	2_AD15
14	2_AD14
13	2_AD13
12	2_AD12
11	2_AD11
10	2_AD10
9	2_AD9
8	2_AD8
7	2_AD7
6	2_AD6
5	2_AD5
4	2_AD4
3	2_AD3
2	2_AD2
1	2_AD1
0	2_AD0

Table 3–10 lists the group definitions for the 2_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-10: 2_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	3_AD31
30	3_AD30
29	3_AD29
28	3_AD28
27	3_AD27
26	3_AD26
25	3_AD25
24	3_AD24

Table 3-10: 2_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
23	3_AD23
22	3_AD22
21	3_AD21
20	3_AD20
19	3_AD19
18	3_AD18
17	3_AD17
16	3_AD16
15	3_AD15
14	3_AD14
13	3_AD13
12	3_AD12
11	3_AD11
10	3_AD10
9	3_AD9
8	3_AD8
7	3_AD7
6	3_AD6
5	3_AD5
4	3_AD4
3	3_AD3
2	3_AD2
1	3_AD1
0	3_AD0

Table 3–11 lists the group definitions for the 1_AD[31:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-11: 1_AD[31:0] channel group definitions

Bit order	AGP 3.0 support channel name
31	1_AD31
30	1_AD30
29	1_AD29
28	1_AD28
27	1_AD27
26	1_AD26
25	1_AD25
24	1_AD24
23	1_AD23
22	1_AD22
21	1_AD21
20	1_AD20
19	1_AD19
18	1_AD18
17	1_AD17
16	1_AD16
15	1_AD15
14	1_AD14
13	1_AD13
12	1_AD12
11	1_AD11
10	1_AD10
9	1_AD9
8	1_AD8
7	1_AD7
6	1_AD6
5	1_AD5
4	1_AD4
3	1_AD3

Table 3-11: 1_AD[31:0] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
2	1_AD2
1	1_AD1
0	1_AD0

Table 3–12 lists the group definitions for the 0/PCI_AD[31] channel group. By default, this group is displayed in hexadecimal.

Table 3-12: 0/PCI_AD[31] channel group definitions

Bit order	AGP 3.0 support channel name
31	0/PCI_AD31
30	0/PCI_AD30
29	0/PCI_AD29
28	0/PCI_AD28
27	0/PCI_AD27
26	0/PCI_AD26
25	0/PCI_AD25
24	0/PCI_AD24
23	0/PCI_AD23
22	0/PCI_AD22
21	0/PCI_AD21
20	0/PCI_AD20
19	0/PCI_AD19
18	0/PCI_AD18
17	0/PCI_AD17
16	0/PCI_AD16
15	0/PCI_AD15
14	0/PCI_AD14
13	0/PCI_AD13
12	0/PCI_AD12
11	0/PCI_AD11
10	0/PCI_AD10

Table 3-12: 0/PCI_AD[31] channel group definitions (Cont.)

Bit order	AGP 3.0 support channel name
9	0/PCI_AD9
8	0/PCI_AD8
7	0/PCI_AD7
6	0/PCI_AD6
5	0/PCI_AD5
4	0/PCI_AD4
3	0/PCI_AD3
2	0/PCI_AD2
1	0/PCI_AD1
0	0/PCI_AD0

Table 3–13 lists the group definitions for the 7_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-13: 7_C#_BE[3:0]channel group definitions

Bit order	AGP 3.0 support channel name
3	7_C#_BE3
2	7_C#_BE2
1	7_C#_BE1
0	7_C#_BE0

Table 3–14 lists the group definitions for the 6_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-14: 6_C#_BE[3:0]channel group definitions

Bit order	AGP 3.0 support channel name
3	6_C#_BE3
2	6_C#_BE2
1	6_C#_BE1
0	6_C#_BE0

Table 3–15 lists the group definitions for the 5_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-15: 5_C#_BE[3:0] channel group definitions

Bit order	AGP 3.0 support channel name
3	5_C#_BE3
2	5_C#_BE2
1	5_C#_BE1
0	5_C#_BE0

Table 3–16 lists the group definitions for the 4_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-16: 4_C#_BE[3:0] channel group definitions

Bit order	AGP 3.0 support channel name
3	4_C#_BE3
2	4_C#_BE2
1	4_C#_BE1
0	4_C#_BE0

Table 3–17 lists the group definitions for the 3_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-17: 3_C#_BE[3:0]channel group definitions

Bit order	AGP 3.0 support channel name
3	3_C#_BE3
2	3_C#_BE2
1	3_C#_BE1
0	3_C#_BE0

Table 3–18 lists the group definitions for the 2_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-18: 2_C#_BE[3:0] channel group definitions

Bit order	AGP 3.0 support channel name
3	2_C#_BE3
2	2_C#_BE2
1	2_C#_BE1
0	2_C#_BE0

Table 3–19 lists the group definitions for the 1_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-19: 1_C#_BE[3:0] channel group definitions

Bit order	AGP 3.0 support channel name
3	1_C#_BE3
2	1_C#_BE2
1	1_C#_BE1
0	1_C#_BE0

Table 3–20 lists the group definitions for the 0/PCI_C#_BE[3:0] channel group. By default, this group is displayed in hexadecimal.

Table 3-20: 0/PCI_C#_BE[3:0] channel group definitions

Bit Order	AGP 3.0 support channel name
3	0 _C#_BE3
2	0_C#_BE2
1	0_C#_BE1
0	0_C#_BE0

Table 3–21 lists the group definitions for the 7_SBA[7:0]# channel group. By default, this group is displayed in hexadecimal.

Table 3-21: 7_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	7_SBA7
6	7_SBA6
5	7_SBA5
4	7_SBA4
3	7_SBA3
2	7_SBA2
1	7_SBA1
0	7_SBA0

Table 3–22 lists the group definitions for the 6_SBA[7:0]# channel group. The symbol table file name is AGP3 _SBA_Cmd. By default, this group is displayed as symbols.

Table 3-22: 6_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	6_SBA7
6	6_SBA6
5	6_SBA5
4	6_SBA4
3	6_SBA3
2	6_SBA2
1	6_SBA1
0	6_SBA0

Table 3–23 lists the group definitions for the 5_SBA[7:0]# channel group. By default, this group is displayed in hexadecimal.

Table 3-23: 5_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	5_SBA7
6	5_SBA6
5	5_SBA5
4	5_SBA4
3	5_SBA3
2	5_SBA2
1	5_SBA1
0	5_SBA0

Table 3–24 lists the group definitions for the 4_SBA[7:0]# channel group. The symbol table file name is AGP3 _SBA_Cmd. By default, this group is displayed as symbols.

Table 3-24: 4_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	4_SBA7
6	4_SBA6
5	4_SBA5
4	4_SBA4
3	4_SBA3
2	4_SBA2
1	4_SBA1
0	4_SBA0

Table 3–25 lists the group definitions for the 3_SBA[7:0]# channel group. By default, this group is displayed in hexadecimal.

Table 3-25: 3_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	3_SBA7
6	3_SBA6
5	3_SBA5
4	3_SBA4
3	3_SBA3
2	3_SBA2
1	3_SBA1
0	3_SBA0

Table 3–26 lists the group definitions for the 2_SBA[7:0]# channel group. The symbol table file name is AGP3 _SBA_Cmd. By default, this group is displayed as symbols.

Table 3-26: 2_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	2_SBA7
6	2_SBA6
5	2_SBA5
4	2_SBA4
3	2_SBA3
2	2_SBA2
1	2_SBA1
0	2_SBA0

Table 3–27 lists the group definitions for the 1_SBA[7:0]# channel group. By default, this group is displayed in hexadecimal.

Table 3-27: 1_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	1_SBA7
6	1_SBA6
5	1_SBA5
4	1_SBA4
3	1_SBA3
2	1_SBA2
1	1_SBA1
0	1_SBA0

Table 3–28 lists the group definitions for the 0/PCI_SBA[7:0]# channel group. The symbol table file name is AGP3 _SBA_Cmd. By default, this group is displayed as symbols.

Table 3-28: 0/PCI_SBA[7:0]# channel group definitions

Bit order	AGP 3.0 support channel name
7	0_SBA7
6	0_SBA6
5	0_SBA5
4	0_SBA4
3	0_SBA3
2	0_SBA2
1	0_SBA1
0	0_SBA0

Table 3–29 lists the group definitions for the Command channel group. The symbol table file name is AGP3 _Command. By default, this group is displayed as symbols.

Table 3-29: Command channel group definitions

Bit order	AGP 3.0 support channel name
7	IRDY
6	FRAME
5	FRAME_L
4	8X/PCI#_AD_D
3	0/PCI_C#_BE3
2	0/PCI_C#_BE2
1	0/PCI_C#_BE1
0	0/PCI_C#_BE0

Table 3–30 lists the group definitions for the Control channel group. The symbol table file name is AGP3_Control. By default, this group is displayed as symbols.

Table 3-30: Control channel group definitions

Bit order	AGP 3.0 support channel name
13	RESET#
12	PME#
11	RBF
10	SERR
9	PERR
8	PAR
7	REQ
6	GNT
5	FRAME
4	FRAME_L
3	IRDY
2	TRDY
1	DEVSEL
0	STOP

Table 3–31 lists the group definitions for the Status channel group. The symbol table file name is AGP3 _Status. By default, this group is displayed as symbols.

Table 3-31: Status channel group definitions

Bit order	AGP 3.0 support channel name
3	GNT
2	ST2
1	ST1
0	ST0

Table 3–32 lists the group definitions for the Misc channel group. By default, this group is displayed as hexadecimal.

Table 3-32: Misc channel group definitions

Bit order	AGP 3.0 support channel name
6	PCI_DBI_HI#
5	PCI_DBI_LO#
4	OVRCNT#
3	RBF
2	WBF
1	INTA#
0	INTB#

Channel Assignment Tables

Channel assignments shown in Tables 3–33 through 3–46 use the following conventions:

- A pound sign (#) following a signal name indicates an active low signal.
- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- An @ sign indicates that this signal is derived on the probe adapter.
- The term master module refers to the middle module of a 3-wide module merge. The term slave module refers to the module in the higher numbered slot than the master module. The term slave 2 module refers to the module in the lower numbered slot than the master module.

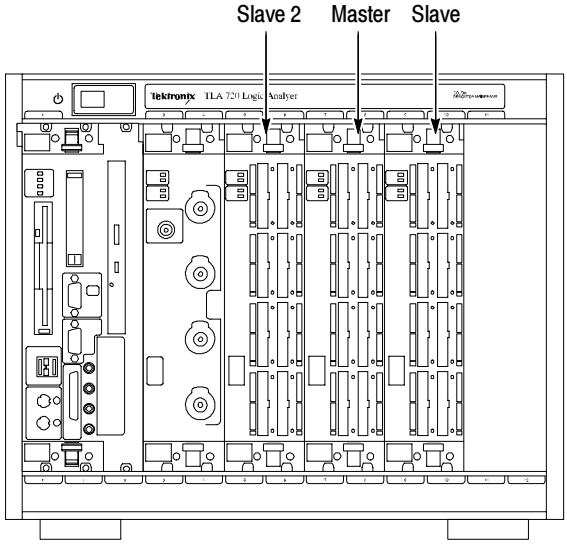

Figure 3-1: Configuration for slave 2, master, and slave modules

Clock Channel Assignments

Table 3–33 lists the clock channel assignments and the corresponding support signal.

Table 3-33: Clock channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
Clock:0	CLK	FRAME
Clock:1	PHASE_D	AD_STBF0
Clock:2	---	CLK
Clock:3	---	SB_STBF
S_Clock:0	PCI_DBI_HI#	---
S_Clock:1	PCI_DBI_LO#	---
S2_Clock:0	TRDY	---
S2_Clock:1	8X/PCI#_AD_D	---
S2_Clock:2	FRAME	---

Qual Channel Assignments

Table 3–34 lists the Qual channel assignments and the corresponding support signal.

Table 3-34: Qual channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
Clock:0	CLK	---
QUAL:1	FRAME_L	AD_STBF1
QUAL:2	Q_RESET#	---
S2_QUAL:0	IRDY	---

Disassembly and Timing Channel Assignments

Table 3–35 lists the channel assignments for the Address group and the corresponding support signal.

Table 3- 35: Master Address Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
A0:0	4_AD16	DEVSEL
A0:1	4_AD17	SERR
A0:2	4_AD18	C#_BE1
A0:3	4_AD19	AD14
A0:4	4_AD20	AD12
A0:5	4_AD21	AD10
A0:6	4_AD22	AD8
A0:7	4_AD23	AD0
A1:0	4_AD24	---
A1:1	4_AD25	AD2
A1:2	4_AD26	AD4
A1:3	4_AD27	AD6
A1:4	4_AD28	AD_STBS0
A1:5	4_AD29	PME#
A1:6	4_AD30	TRDY
A1:7	4_AD31	AD16
A2:0	5_AD16	IRDY
A2:1	5_AD17	PERR
A2:2	5_AD18	C#_BE2
A2:3	5_AD19	AD7
A2:4	5_AD20	AD5
A2:5	5_AD21	AD3
A2:6	5_AD22	AD1
A2:7	5_AD23	---
A3:0	5_AD24	C#_BE0
A3:1	5_AD25	AD9
A3:2	5_AD26	AD11
A3:3	5_AD27	AD13

Table 3-35: Master Address Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
A3:4	5_AD28	AD15
A3:5	5_AD29	PAR
A3:6	5_AD30	STOP
A3:7	5_AD31	---

Table 3–36 lists the channel assignments for the Control group and the corresponding support signal.

Table 3-36: Master Control Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
C0:0	6_AD16	---
C0:1	6_AD17	SBA4#
C0:2	6_AD18	SBA6#
C0:3	6_AD19	AD31
C0:4	6_AD20	AD29
C0:5	6_AD21	AD27
C0:6	6_AD22	AD25
C0:7	6_AD23	---
C1:0	6_AD24	---
C1:1	6_AD25	AD24
C1:2	6_AD26	AD26
C1:3	6_AD27	AD28
C1:4	6_AD28	AD30
C1:5	6_AD29	SBA7#
C1:6	6_AD30	SBA5#
C1:7	6_AD31	SB_STBS
C2:0	7_AD16	SBA0#

Table 3-36: Master Control Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
C2:1	7_AD17	SBA2#
C2:2	7_AD18	---
C2:3	7_AD19	AD23
C2:4	7_AD20	AD21
C2:5	7_AD21	AD19
C2:6	7_AD22	AD17
C2:7	7_AD23	---
C3:0	7_AD24	---
C3:1	7_AD25	---
C3:2	7_AD26	AD18
C3:3	7_AD27	AD20
C3:4	7_AD28	AD22
C3:5	7_AD29	C#_BE3
C3:6	7_AD30	AD_STBS1
C3:7	7_AD31	SBA3#

Table 3–37 lists the channel assignments for the Data group and the corresponding support signal.

Table 3-37: Master Data Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
D0:0	4_AD0	---
D0:1	4_AD1	---
D0:2	4_AD2	---
D0:3	4_AD3	---
D0:4	4_AD4	---
D0:5	4_AD5	---

Table 3-37: Master Data Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name	AGP3_T support channel name
D0:6	4_AD6	---
D0:7	4_AD7	---
D1:0	4_AD8	---
D1:1	4_AD9	---
D1:2	4_AD10	---
D1:3	4_AD11	WBF
D1:4	4_AD12	ST1
D1:5	4_AD13	RESET#
D1:6	4_AD14	USB-
D1:7	4_AD15	TYPEDET#
D2:0	5_AD0	SBA1#
D2:1	5_AD1	DBI_LO
D2:2	5_AD2	RBF
D2:3	5_AD3	ST0
D2:4	5_AD4	INTB#
D2:5	5_AD5	OVRCNT#
D2:6	5_AD6	---
D2:7	5_AD7	---
D3:0	5_AD8	USB+
D3:1	5_AD9	REQ
D3:2	5_AD10	ST2
D3:3	5_AD11	DBI_HI
D3:4	5_AD12	MB_DET#
D3:5	5_AD13	GNT
D3:6	5_AD14	INTA#
D3:7	5_AD15	GC_DET#

Table 3–38 lists the channel assignments for the Extend group and the corresponding support signal.

Table 3-38: Master Extend Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
E0:0	6_AD0
E0:1	6_AD1
E0:2	6_AD2
E0:3	6_AD3
E0:4	6_AD4
E0:5	6_AD5
E0:6	6_AD6
E0:7	6_AD7
E1:0	6_AD8
E1:1	6_AD9
E1:2	6_AD10
E1:3	6_AD11
E1:4	6_AD12
E1:5	6_AD13
E1:6	6_AD14
E1:7	6_AD15
E2:0	7_AD0
E2:1	7_AD1
E2:2	7_AD2
E2:3	7_AD3
E2:4	7_AD4
E2:5	7_AD5
E2:6	7_AD6
E2:7	7_AD7
E3:0	7_AD8
E3:1	7_AD9
E3:2	7_AD10
E3:3	7_AD11

Table 3-38: Master Extend Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
E3:4	7_AD12
E3:5	7_AD13
E3:6	7_AD14
E3:7	7_AD15

Table 3–39 lists the channel assignments for the Slave Address group and the corresponding support signal.

Table 3-39: Slave Address Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_A0:0	4_C#_BE0
S_A0:1	4_C#_BE1
S_A0:2	4_C#_BE2
S_A0:3	4_C#_BE3
S_A0:4	5_C#_BE0
S_A0:5	5_C#_BE1
S_A0:6	5_C#_BE2
S_A0:7	5_C#_BE3
S_A1:0	6_C#_BE0
S_A1:1	6_C#_BE1
S_A1:2	6_C#_BE2
S_A1:3	6_C#_BE3
S_A1:4	7_C#_BE0
S_A1:5	7_C#_BE1
S_A1:6	7_C#_BE2
S_A1:7	7_C#_BE3
S_A2:0	1_AD16
S_A2:1	1_AD17
S_A2:2	1_AD18

Table 3-39: Slave Address Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_A2:3	1_AD19
S_A2:4	1_AD20
S_A2:5	1_AD21
S_A2:6	1_AD22
S_A2:7	1_AD23
S_A3:0	1_AD24
S_A3:1	1_AD25
S_A3:2	1_AD26
S_A3:3	1_AD27
S_A3:4	1_AD28
S_A3:5	1_AD29
S_A3:6	1_AD30
S_A3:7	1_AD31

Table 3–40 lists the channel assignments for the Slave Control group and the corresponding support signal.

Table 3-40: Slave Control Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_C0:0	2_AD16
S_C0:1	2_AD17
S_C0:2	2_AD18
S_C0:3	2_AD19
S_C0:4	2_AD20
S_C0:5	2_AD21
S_C0:6	2_AD22
S_C0:7	2_AD23
S_C1:0	2_AD24
S_C1:1	2_AD25

Table 3-40: Slave Control Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_C1:2	2_AD26
S_C1:3	2_AD27
S_C1:4	2_AD28
S_C1:5	2_AD29
S_C1:6	2_AD30
S_C1:7	2_AD31
S_C2:0	3_AD16
S_C2:1	3_AD17
S_C2:2	3_AD18
S_C2:3	3_AD19
S_C2:4	3_AD20
S_C2:5	3_AD21
S_C2:6	3_AD22
S_C2:7	3_AD23
S_C3:0	3_AD24
S_C3:1	3_AD25
S_C3:2	3_AD26
S_C3:3	3_AD27
S_C3:4	3_AD28
S_C3:5	3_AD29
S_C3:6	3_AD30
S_C3:7	3_AD31

Table 3–41 lists the channel assignments for the Slave Data group and the corresponding support signal.

Table 3- 41: Slave Data Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_D0:0	0/PCI_C#_BE0
S_D0:1	0/PCI_C#_BE1
S_D0:2	0/PCI_C#_BE2
S_D0:3	0/PCI_C#_BE3
S_D0:4	1_C#_BE0
S_D0:5	1_C#_BE1
S_D0:6	1_C#_BE2
S_D0:7	1_C#_BE3
S_D1:0	2_C#_BE0
S_D1:1	2_C#_BE1
S_D1:2	2_C#_BE2
S_D1:3	2_C#_BE3
S_D1:4	3_C#_BE0
S_D1:5	3_C#_BE1
S_D1:6	3_C#_BE2
S_D1:7	3_C#_BE3
S_D2:0	1_AD0
S_D2:1	1_AD1
S_D2:2	1_AD2
S_D2:3	1_AD3
S_D2:4	1_AD4
S_D2:5	1_AD5
S_D2:6	1_AD6
S_D2:7	1_AD7
S_D3:0	1_AD8
S_D3:1	1_AD9
S_D3:2	1_AD10
S_D3:3	1_AD11

Table 3-41: Slave Data Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_D3:4	1_AD12
S_D3:5	1_AD13
S_D3:6	1_AD14
S_D3:7	1_AD15

Table 3–42 lists the channel assignments for the Slave Extend group and the corresponding support signal.

Table 3-42: Slave Extend Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_E0:0	2_AD0
S_E0:1	2_AD1
S_E0:2	2_AD2
S_E0:3	2_AD3
S_E0:4	2_AD4
S_E0:5	2_AD5
S_E0:6	2_AD6
S_E0:7	2_AD7
S_E1:0	2_AD8
S_E1:1	2_AD9
S_E1:2	2_AD10
S_E1:3	2_AD11
S_E1:4	2_AD12
S_E1:5	2_AD13
S_E1:6	2_AD14
S_E1:7	2_AD15
S_E2:0	3_AD0
S_E2:1	3_AD1
S_E2:2	3_AD2

Table 3-42: Slave Extend Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S_E2:3	3_AD3
S_E2:4	3_AD4
S_E2:5	3_AD5
S_E2:6	3_AD6
S_E2:7	3_AD7
S_E3:0	3_AD8
S_E3:1	3_AD9
S_E3:2	3_AD10
S_E3:3	3_AD11
S_E3:4	3_AD12
S_E3:5	3_AD13
S_E3:6	3_AD14
S_E3:7	3_AD15

Table 3–43 lists the channel assignments for the Slave2 Address group and the corresponding support signal.

Table 3-43: Slave2 Address Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_A0:0	0/PCI_AD0
S2_A0:1	0/PCI_AD1
S2_A0:2	0/PCI_AD2
S2_A0:3	0/PCI_AD3
S2_A0:4	0/PCI_AD4
S2_A0:5	0/PCI_AD5
S2_A0:6	0/PCI_AD6
S2_A0:7	0/PCI_AD7

Table 3-43: Slave2 Address Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_A1:0	0/PCI_AD8
S2_A1:1	0/PCI_AD9
S2_A1:2	0/PCI_AD10
S2_A1:3	0/PCI_AD11
S2_A1:4	0/PCI_AD12
S2_A1:5	0/PCI_AD13
S2_A1:6	0/PCI_AD14
S2_A1:7	0/PCI_AD15
S2_A2:0	0/PCI_AD16
S2_A2:1	0/PCI_AD17
S2_A2:2	0/PCI_AD18
S2_A2:3	0/PCI_AD19
S2_A2:4	0/PCI_AD20
S2_A2:5	0/PCI_AD21
S2_A2:6	0/PCI_AD22
S2_A2:7	0/PCI_AD23
S2_A3:0	0/PCI_AD24
S2_A3:1	0/PCI_AD25
S2_A3:2	0/PCI_AD26
S2_A3:3	0/PCI_AD27
S2_A3:4	0/PCI_AD28
S2_A3:5	0/PCI_AD29
S2_A3:6	0/PCI_AD30
S2_A3:7	0/PCI_AD31

Table 3–44 lists the channel assignments for the Slave2 Control group and the corresponding support signal.

Table 3- 44: Slave2 Control Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_C0:0	4_SBA0#
S2_C0:1	4_SBA1#
S2_C0:2	4_SBA2#
S2_C0:3	4_SBA3#
S2_C0:4	4_SBA4#
S2_C0:5	4_SBA5#
S2_C0:6	4_SBA6#
S2_C0:7	4_SBA7#
S2_C1:0	5_SBA0#
S2_C1:1	5_SBA1#
S2_C1:2	5_SBA2#
S2_C1:3	5_SBA3#
S2_C1:4	5_SBA4#
S2_C1:5	5_SBA5#
S2_C1:6	5_SBA6#
S2_C1:7	5_SBA7#
S2_C2:0	6_SBA0#
S2_C2:1	6_SBA1#
S2_C2:2	6_SBA2#
S2_C2:3	6_SBA3#
S2_C2:4	6_SBA4#
S2_C2:5	6_SBA5#
S2_C2:6	6_SBA6#
S2_C2:7	6_SBA7#
S2_C3:0	7_SBA0#
S2_C3:1	7_SBA1#
S2_C3:2	7_SBA2#
S2_C3:3	7_SBA3#

Table 3-44: Slave2 Control Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_C3:4	7_SBA4#
S2_C3:5	7_SBA5#
S2_C3:6	7_SBA6#
S2_C3:7	7_SBA7#

Table 3–45 lists the channel assignments for the Slave2 Data group and the corresponding support signal.

Table 3-45: Slave2 Data Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_D0:0	INTA#
S2_D0:1	USB_NEG
S2_D0:2	GC_DET
S2_D0:3	TYPEDET#
S2_D0:5	DEVSEL
S2_D0:6	PERR
S2_D0:7	SERR
S2_D1:0	PAR
S2_D1:1	PME#
S2_D1:2	STOP
S2_D2:0	RESET#
S2_D2:1	GNT
S2_D2:2	ST1
S2_D2:3	MB_DET#
S2_D2:4	WBF
S2_D2:5	RBF
S2_D2:6	ST2
S2_D2:7	ST0
S2_D3:0	REQ

Table 3-45: Slave2 Data Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_D3:1	INTB#
S2_D3:2	USB_POS
S2_D3:3	OVRCNT#

Table 3–46 lists the channel assignments for the Slave2 Extend group and the corresponding support signal.

Table 3-46: Slave2 Extend Module 32-channel assignments

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_E0:0	0/PCI_SBA0#
S2_E0:1	0/PCI_SBA1#
S2_E0:2	0/PCI_SBA2#
S2_E0:3	0/PCI_SBA3#
S2_E0:4	0/PCI_SBA4#
S2_E0:5	0/PCI_SBA5#
S2_E0:6	0/PCI_SBA6#
S2_E0:7	0/PCI_SBA7#
S2_E1:0	1_SBA0#
S2_E1:1	1_SBA1#
S2_E1:2	1_SBA2#
S2_E1:3	1_SBA3#
S2_E1:4	1_SBA4#
S2_E1:5	1_SBA5#
S2_E1:6	1_SBA6#
S2_E1:7	1_SBA7#
S2_E2:0	2_SBA0#
S2_E2:1	2_SBA1#
S2_E2:2	2_SBA2#
S2_E2:3	2_SBA3#

Table 3-46: Slave2 Extend Module 32-channel assignments (Cont.)

Logic analyzer acquisition channel	AGP 3.0 support channel name
S2_E2:4	2_SBA4#
S2_E2:5	2_SBA5#
S2_E2:6	2_SBA6#
S2_E2:7	2_SBA7#
S2_E3:0	3_SBA0#
S2_E3:1	3_SBA1#
S2_E3:2	3_SBA2#
S2_E3:3	3_SBA3#
S2_E3:4	3_SBA4#
S2_E3:5	3_SBA5#
S2_E3:6	3_SBA6#
S2_E3:7	3_SBA7#

Signals Required for Clocking and Disassembly

The following is a list of the AGP 3.0 bus signals required by the Clocking State Machine (CSM) and disassembler to properly strobe and login the bus cycles into acquisition memory, and to disassemble the acquired bus cycles. Signals acquired as data but not required for clocking are not included. Signals required for any probe adapter circuitry are included, if that circuitry is required for clocking.

0_SBA[7:0]# @	RESET#	FRAME_L
2_SBA[7:0]# @	AD_STBF1	
4_SBA[7:0]# @	AD_STBS1	
6_SBA[7:0]# @	AD_STBF0	
PHASE_D @	AD_STBS0	
FRAME	SBA_STBF	
IRDY	SBA_STBS	
TRDY	RBF	
GNT	WBF	
CLK	8X/PCI#_AD_D	

NOTE. *Many of the signals in this table are used to derive PHASE_D and 8X/PCI#_AD_D.*

Specifications

Specifications

This section contains information regarding the specifications of the TMS809 AGP 3.0 bus support package.

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a target system. Table 4–1 lists the electrical requirements the target system must produce for the support to acquire correct data. Table 4–2 lists the timing support channel–to–channel skew requirements. Table 4–3 lists the electrical requirements for the AC power supply. Table 4–4 lists the environmental specifications for the probe adapter.

Table 4-1: Electrical specifications

Characteristics	Requirements
Target system clock rate	Maximum 66 MHz
Target system tested clock rate	Maximum 66.5 MHz
Common clock capture	
T_{su}	375 ps
T_{hd}	-25 ps
Source Synchronous capture (Backside probe adapter)	
T_{su}	185 ps
T_{hd}	265 ps
Source Synchronous capture (Interposer probe adapter)	
T_{su}	220 ps
T_{hd}	325 ps
Input Swigs (Source Synchronous signals)	
V_{IH}	600 mV
V_{IL}	100 mV

Figure 4–1 shows the strobe separation requirements for the allowable time skew between the falling edge of the STBF signal and the rising edge of the STBS signal.

The rising edge of the STBS signal must not occur more than 250 ps before or more than 870 ps after the falling edge of the STBF. These specifications apply to all three strobe pairs.

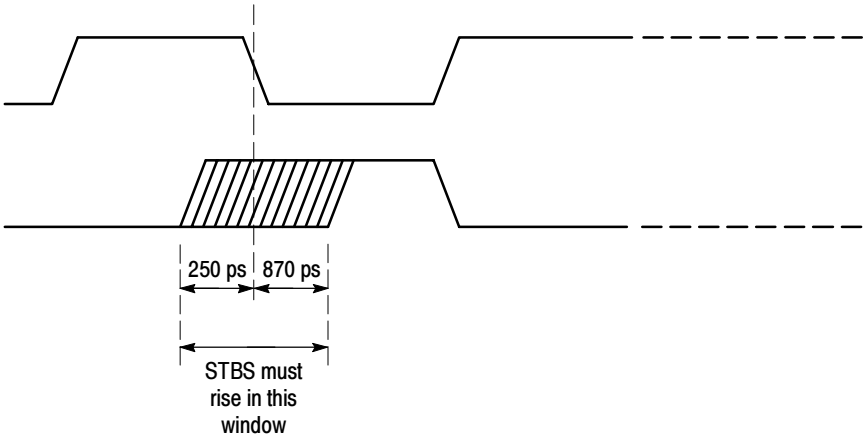

Figure 4-1: Strobe separation

All channels at the timing support connectors have the same timing relationship to one another as they do on the target system with the exception of the channels listed in Table 4–2. These timing misalignments do not affect state acquisition. All skew characteristics are typical values.

A positive number means the signal occurs later than the nonskewed signals and a negative number means the signal occurs earlier than the nonskewed signals.

Table 4-2: Timing Support Channel-to-Channel Skew

AGP3_T support channel name	Skew
CLK	+ 0.37 Ns
RESET#	+/– 1.0 Ns
SB_STBF	+ 0.1 Ns

Table 4-3: Electrical specifications for the AC input

Characteristic	Description
Input Voltage rating	100 - 240 VAC CAT II
Input Frequency Rating	50 - 60 Hz
Input Current Rating	6.0 A maximum

Table 4-4: Environmental specifications

Characteristic	Description[1]
Temperature	
Maximum operating	+50 °C (+122 °F)[2]
Minimum operating	0 °C (+32 °F)
Non operating	-55 °C to +75 °C (-67 ° to +167 °F)
Humidity	10 to 95% relative humidity, noncondensing
Altitude	
Operating	3000 m (10,000 ft) maximum
Non operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive
Required airflow clearances (preprocessor unit)	10 to 95% relative humidity, noncondensing
Sides	2 in (5.08 cm)
Back	3 in (7.62 cm)

1 Designed to meet Tektronix standard 062-2847-00 class 5.

2 Not to exceed AGP 3.0 bus thermal considerations. Forced air cooling is required.

CAUTION. *To prevent damage to the circuitry in the preprocessor unit, you must observe the required clearances in Table 4-4.*

Load Models

Figure 4–2 shows the load model for the Interposer source sync circuit.

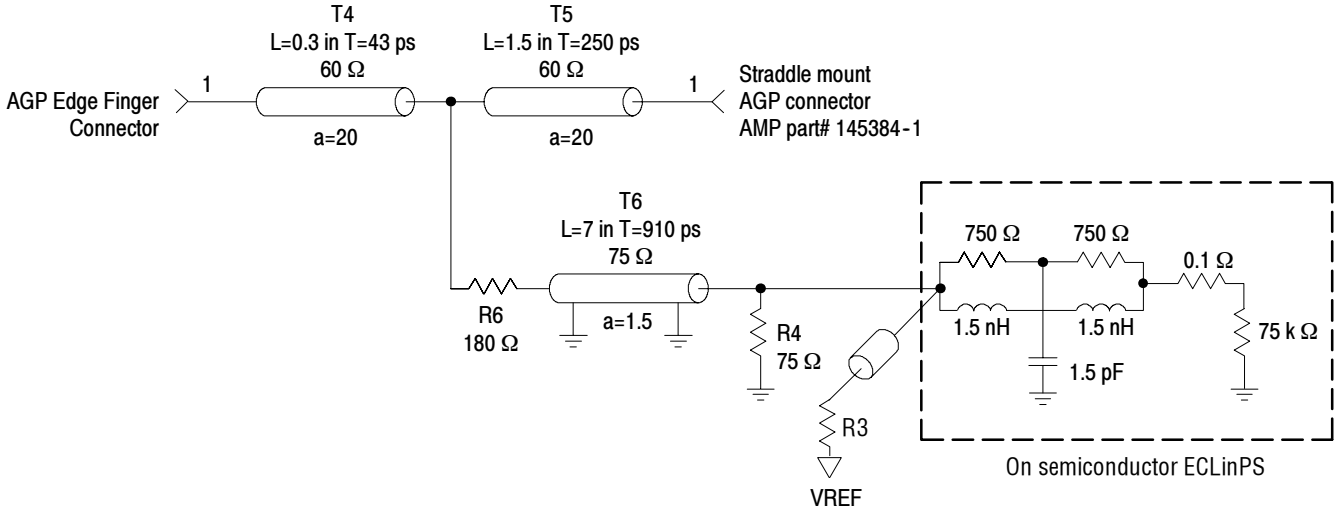

Figure 4-2: Interposer source sync load model

Figure 4–3 shows the load model for the Backside source sync circuit.

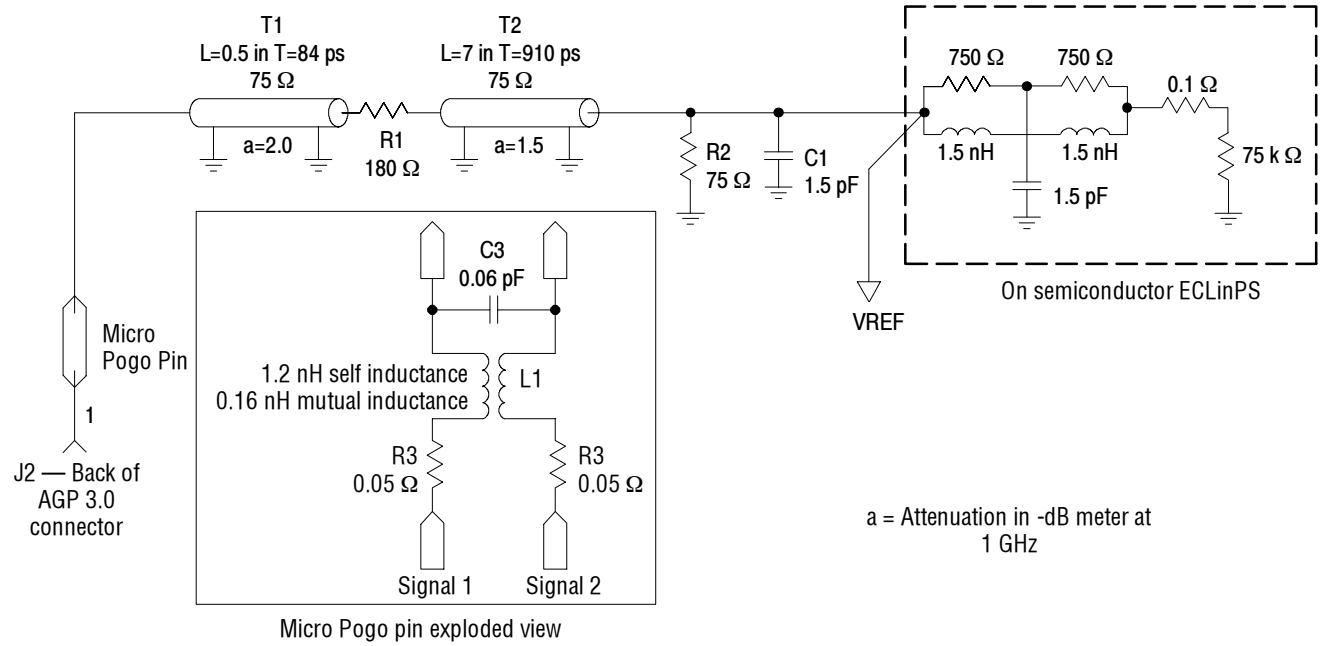

Figure 4-3: Backside source sync load model

Table 4–5 lists the certifications and compliances for the TMS809 AGP 3.0 bus support package.

Table 4-5: Certifications and compliances

Category	Standards or description	
EC Declaration of Conformity — EMC	Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:	
	EN 61000-3-2	AC power line harmonic emissions
EC Declaration of Conformity — Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities:	
	Low Voltage Directive 73/23/EEC, amended by 93/68/EEC	
	EN 61010-1/A2:1995	Safety requirements for electrical equipment for measurement control and laboratory use.
U.S. Nationally Recognized Testing Laboratory Listing	UL3111-1	Standard for electrical measuring and test equipment.
Canadian Certification	CAN/CSA C22.2 No. 1010.1	Safety requirements for electrical equipment for measurement, control, and laboratory use.
Additional Compliance	IEC61010-1/A2:1995	Safety requirements for electrical equipment for measurement, control, and laboratory use.
Installation (Overvoltage) Category Descriptions	Terminals on this product may have different installation (overvoltage) category designations. The installation categories are:	
	CAT III	Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location.
	CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.
	CAT I	Secondary (signal level) or battery operated circuits of electronic equipment.
Pollution Degree Descriptions	A measure of the contaminates that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated.	
	Pollution Degree 1	No pollution or only dry, nonconductive pollution occurs. Products in this category are generally encapsulated, hermetically sealed, or located in clean rooms.
	Pollution Degree 2	Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service.
	Pollution Degree 3	Conductive pollution, or dry, nonconductive pollution that becomes conductive due to condensation. These are sheltered locations where neither temperature nor humidity is controlled. The area is protected from direct sunshine, rain, or direct wind.
	Pollution Degree 4	Pollution that generates persistent conductivity through conductive dust, rain, or snow. Typical outdoor locations.

Table 4-5: Certifications and compliances (Cont.)

Category	Standards or description
Equipment Type	Test and measuring
Safety Class	Class 1 (as defined in IEC 61010-1, Annex H) - grounded product
Overvoltage Category	Overvoltage Category II (as defined in IEC 61010-1, Annex J)
Pollution Degree	Pollution Degree 2 (as defined in IEC 61010-1). Note: Rated for indoor use only.

Dimensions Figure 4–4 shows the dimensions of the AGP 3.0 Interposer probe head.

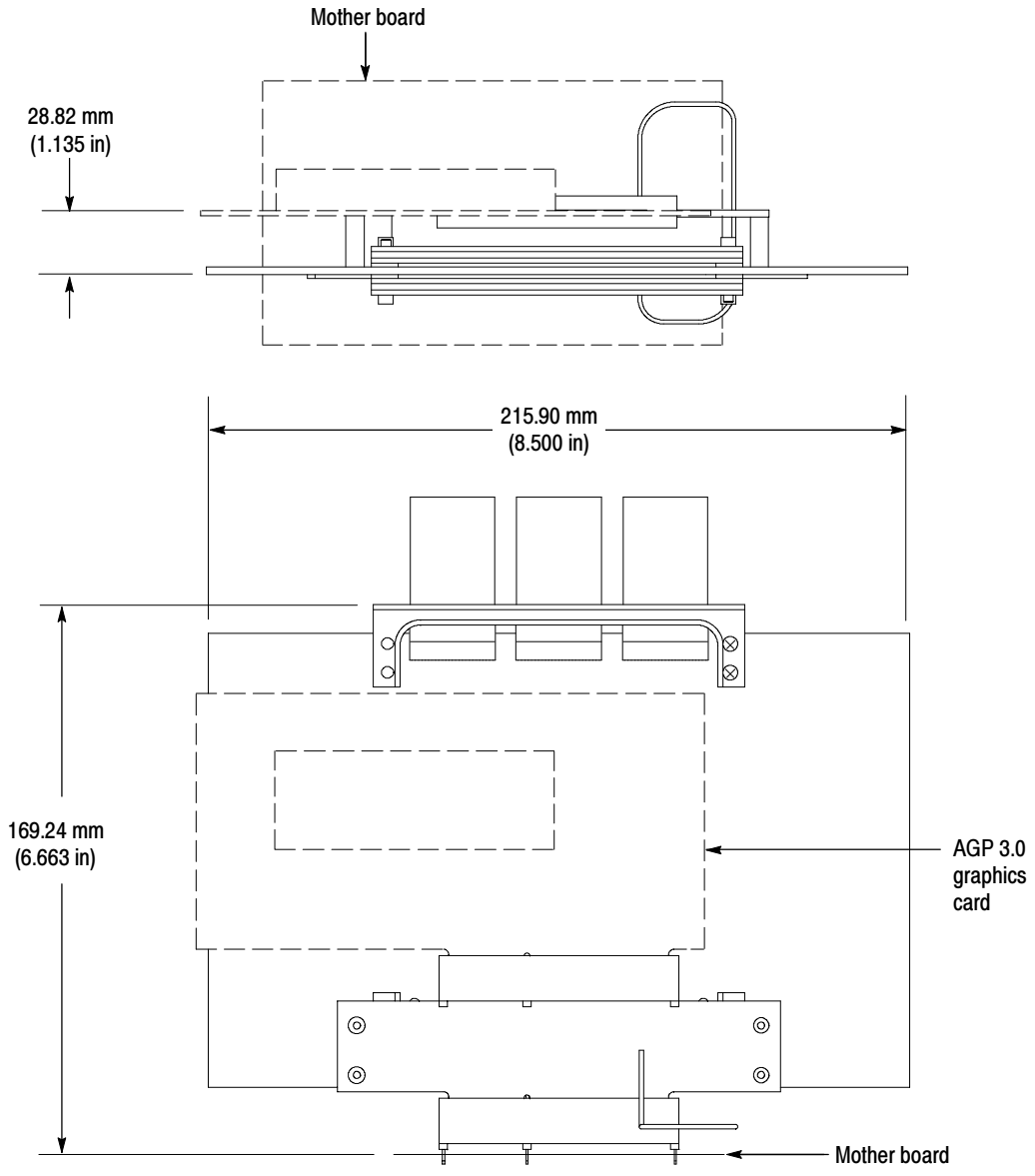

Figure 4- 4: Dimensions of the AGP 3.0 Interposer probe head

Figure 4–5 shows the dimensions of the AGP 3.0 Backside probe head.

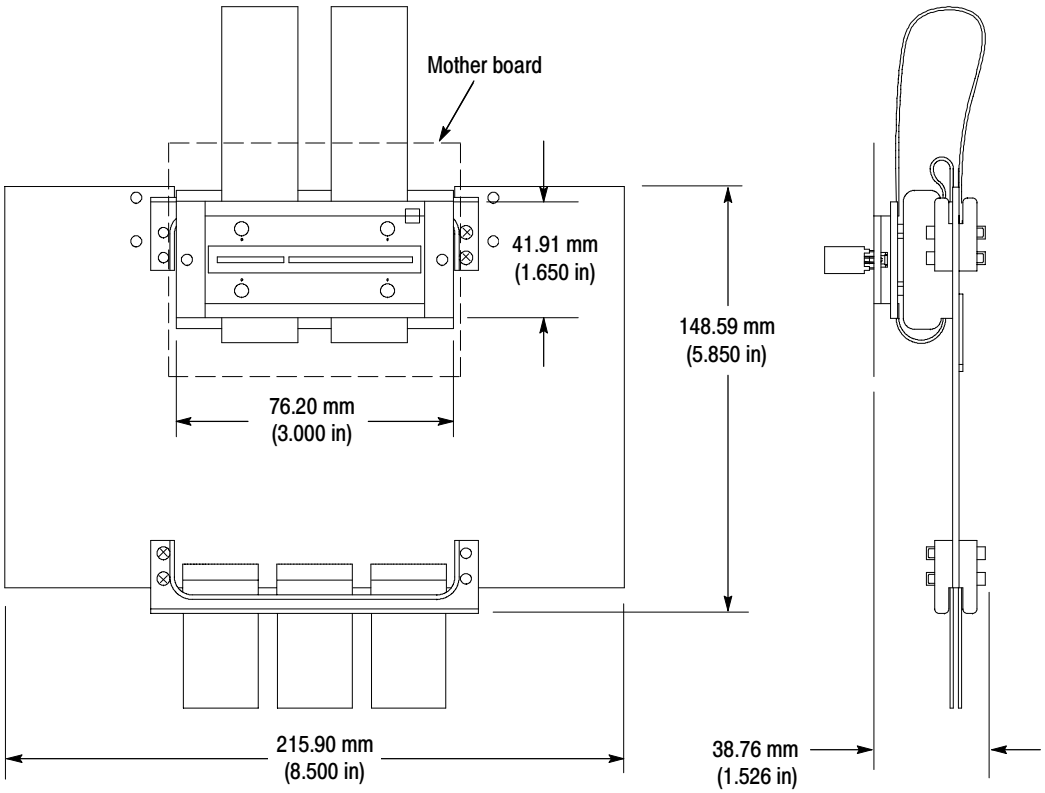

Figure 4- 5: Dimensions of the AGP 3.0 Backside probe head

Figure 4–6 shows the dimensions of the preprocessor unit.

CAUTION. *To prevent damage to the circuitry in the preprocessor unit, you must observe the required clearances in Table 4–4 on page 4–3.*

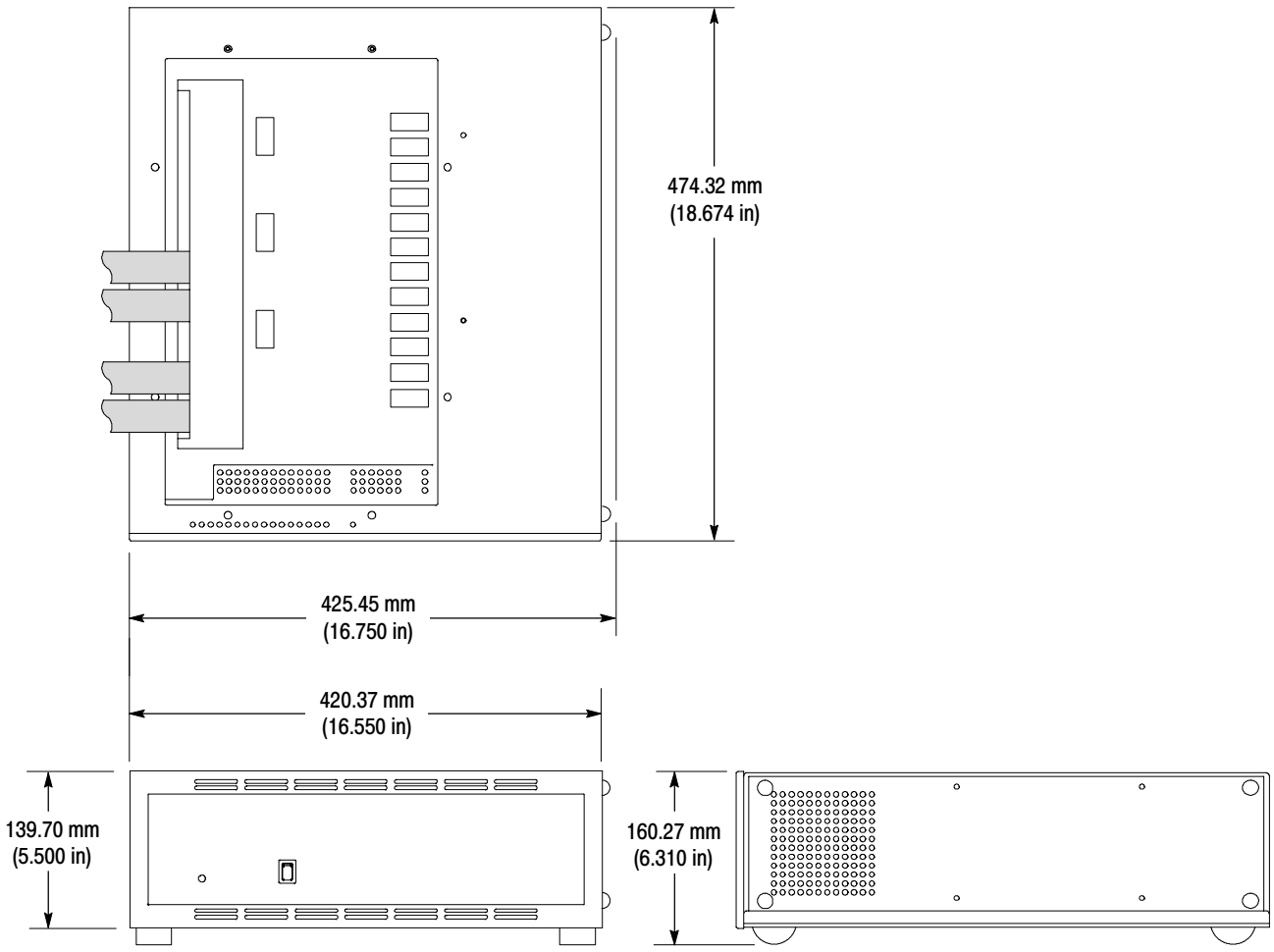

Figure 4- 6: Dimensions of the preprocessor unit

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all safety summaries before performing any service.

Maintenance

Maintenance

This section contains fuse information for the TMS809 AGP 3.0 probe adapter.

The TMS809 AGP 3.0 probe adapter does not require scheduled or periodic maintenance. However, to keep good electrical contact and efficient heat dissipation, keep the probe adapter free of dirt, dust, and contaminants. When not in use, store the probe adapter in the original shipping bags and shipping cartons (see *Storage* on page 1–26)**.**

For information on exterior cleaning of the probe adapter, see *Care and Maintenance* on page 1–27.

WARNING. *To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit. There are no operator serviceable parts inside the cover of the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

Fuses

The fuses for the TMS809 AGP 3.0 probe adapter are located in the preprocessor unit. See the *Replaceable Parts List* for the part numbers.

- In the power supply, there is one fuse:

  10 A, 250 V Fast blow (part number not available)

- On the Logic board there are seven fuses:

  5 A, 125 V Fast blow (5)

  10 A, 125 V Fast blow (2)

Fan Removal and Installation Procedure

This section contains fan removal and installation procedures for the TMS809 probe adapter.

The information in this section is designed for use by qualified service personnel. Read the Safety Summaries at the front of this manual before attempting any procedures in this section.

WARNING. *To prevent harm to yourself or damage to the preprocessor unit, do not open the preprocessor unit, except for fan removal. There are no operator serviceable parts inside the cover of the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

Removing and Instaling a Fan

Read the following general instructions before removing parts.

If all three fans are not working, check that the power cord is connected to the preprocessor unit or the electrical outlet. If the power cord is connected, contact a Tektronix service representative.

CAUTION. *Static discharge can damage the bus, the probe adapter, the probes, and the module. To prevent static damage, handle components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the bus and probe adapter.

Tools Required

Following are the tools required for the removal procedure:

- POZIDRIV screwdriver (PZ1) (to remove bottom cover and fan deflector shield)
- Flat bladed screwdriver (if needed to loosen the screws on the small boards or remove the rivets from a fan guard)
- Dental pick or tweezers (for removing a fan pin from the fan connector)

Removing a Fan

You may need to remove and install a fan in the preprocessor unit for repair purposes. Follow these steps to remove a fan:

1. Power off the preprocessor unit. The power switch is located on the back of the preprocessor unit (see Figure 5-1).
2. Disconnect the P6434 probes. To disconnect the P6434 probes, refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications.
3. Unplug the AC power cord from the preprocessor unit.

Figure 5-1: Power switch and AC power cord locations

WARNING. *To prevent serious injury or death, check that the power cord is disconnected from the preprocessor unit.*

4. Turn the preprocessor over (P6434 probes must have been removed).

5. Remove the screws (see Figure 5–2) from the bottom cover of the preprocessor unit. Set the bottom cover aside.

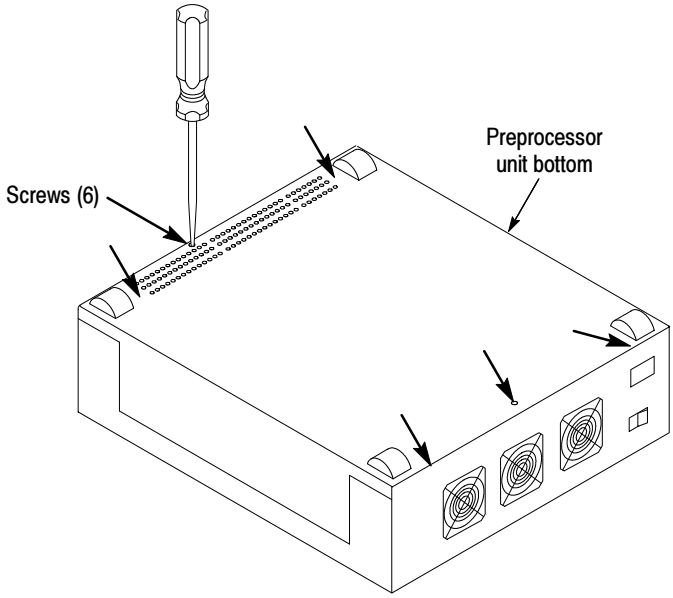

Figure 5–2: Remove the attaching screws

6. If you are replacing the fan behind the power supply, you must first remove the deflector shield that covers the power supply (see Figure 5–3). If not, skip to step 7.

WARNING. *To prevent serious injury or death, check that the power cord is disconnected from the preprocessor unit.*

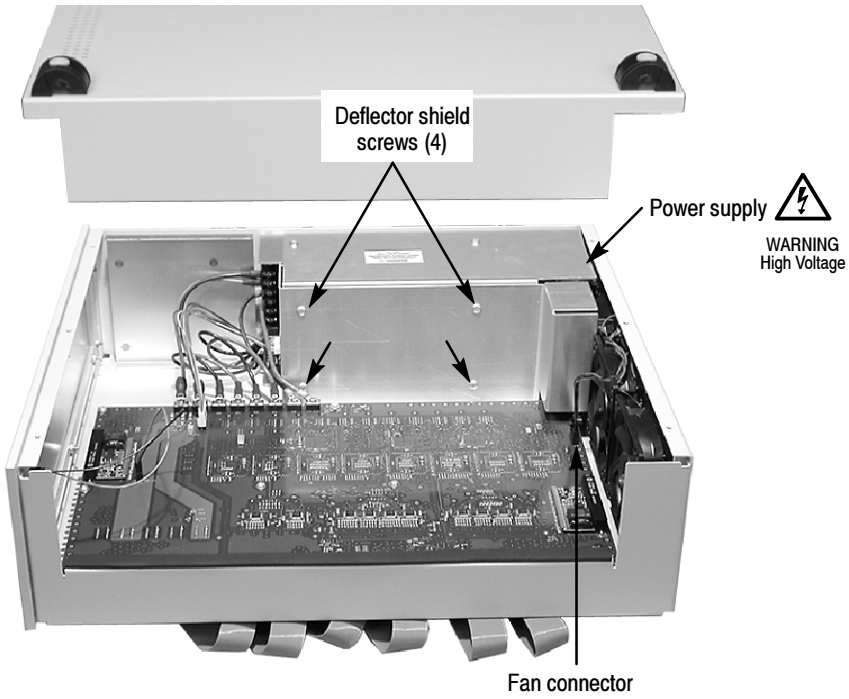

Figure 5–3: Remove the bottom cover

7. Disconnect the fan connector from the logic-board connector (see Figure 5–3) by pressing the release tab on the fan connector.
8. Cut the two cable ties that bundle the fan wires together.

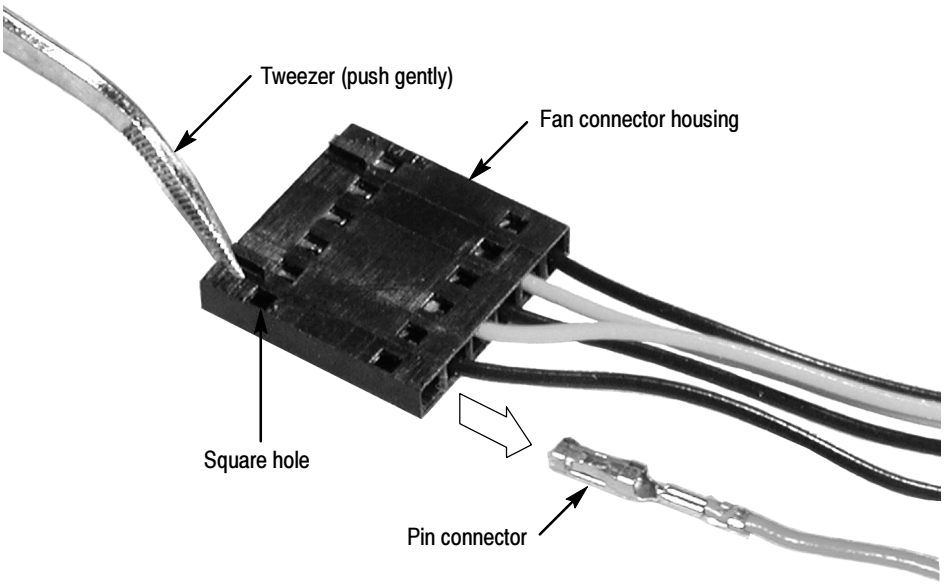

Figure 5-4: Removing the fan pin connector

9. Remove the fan pin from the fan connector housing (at the Logic board connector side) by following steps a through c:

a. Using a dental pick (or tweezer point), place the tool point in the top square hole of the fan connector housing (see Figure 5-4).

b. Gently press and slide the pin a little with the tool point. This small movement releases the pin from the fan connector housing.

CAUTION. *To prevent damage to the fan pin and the fan connector, do not gouge the pin with the tool point.*

c. Gently slide the pin from the fan connector housing using your hand. The pin removal procedure may take a couple of tries, unless you are experienced with pin removal.

10. Remove the rivets, fan guard, and fan from the preprocessor unit. When removing the rivets, pull the rivet pin halfway out and then remove the whole rivet assembly.

11. Remove the fan from the preprocessor unit.

Installing a Fan

1. Position the writing on the fan hub to point toward the back of the preprocessor unit.
2. With the rivet pin pulled halfway out of the rivet assembly, insert the rivet assembly through the fan grill mounting ring, preprocessor hole, and fan hole (see Figure 5-5).

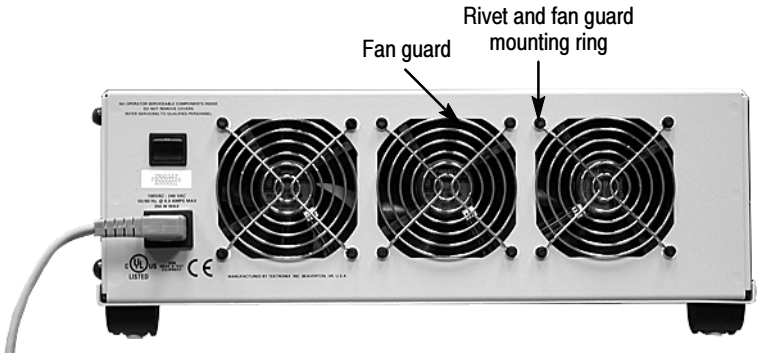

Figure 5-5: Back of the preprocessor unit

***NOTE**. To prevent loose rivet connections, replace the rivets after a couple of removal and replacement operations.*

3. Press the rivet pin into the rivet assembly.
4. Repeat steps 2 and 3 for the other rivet installations.
5. Slide and snap the fan pin into the fan connector housing. Gently pull on the fan pin to insure the fan pin has seated in the fan connector.
6. Connect the fan connector to the Logic-board connector (see Figure 5-3 on page 5-6).

7. Dress the fan wire over the top of the fans and through the notch on the top of the center fan (see Figure 5–6).

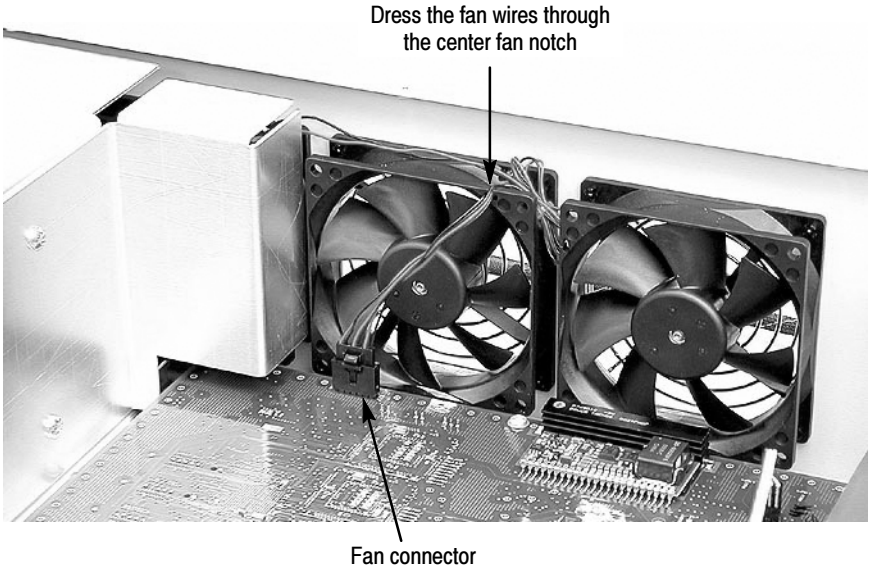

Figure 5–6: Location of fan connector

8. Attach two cable ties to the bundle of fan wires securing the fan wires in place.
9. Attach the bottom cover to the preprocessor unit using the attaching screws, torque to 4 in /lbs (see Figure 5–2 on page 5–5).
10. Turn the preprocessor unit right-side up.
11. Plug the AC power cord into the preprocessor unit.
12. Power on the preprocessor unit and check that the fans are rotating.
13. Attach the P6434 probes (see page 1–20).

If the replaced fan is not working:

- Check that the fan pin is seated properly in the fan connector housing.
- Check that the fan connector has snapped into place.

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components or modules for the TMS809 probe adapter.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-833-9200. Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices: www.tektronix.com.

Module Repair and Return. You may ship your module to us for repair, after which we will return it to you.

New Modules. You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the TMS809 AGP 3.0 probe adapter. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214-4657
30161	AAVID ENGINEERING, INC.	PO BOX 400	LACONIA, NH 03247-0400
5Y400	TRIAX METAL PRODUCTS INC	1880 SW MERLO DRIVE	BEAVERTON, OR 97006
TK0588	UNIVERSAL PRECISION PRODUCT	1775 NW CORNELIUS PASS RD	HILLSBORO, OR 97124
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005
06915	RICHCO	5825 N TRIPP AVE P.O. BOX 804238	CHICAGO, IL 60646
0ADN8	DELTA PRODUCTS CORP-DPZ	4405 CUSHING PARKWAY	FREMONT, CA 94538
0D1M6	NMB TECHNOLOGIES INC	9730 INDEPENDENCE AVE	CHATSWORTH, CA 91311
1AW87	LEWIS SCREW CO.	4300 SOUTH RACINE AVENUE	CHICAGO, IL 60609
26742	METHODE ELECTRONICS INC	7444 WEST WILSON AVE	CHICAGO, IL 60656-4548
2K262	BOYD CORPORATION	6136 NE 87TH AVENUE	PORTLAND, OR 97220
54407	POWER-ONE INC	740 CALLE PLANO	CAMARILLO, CA 93010
5Y400	TRIAX METAL PRODUCTS INC	1880 SW MERLO DRIVE	BEAVERTON, OR 97006
61058	PANASONIC INDUSTRIAL CO ECG	M/S 7H-4 TWO PANASONIC WAY	SECAUCUS, NJ 07094
61857	SAN-O INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK, NY 11741
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES, IL 60016-3049
7W718	MARQUARDT SWITCHES	2711 ROUTE 20 EAST	CAZENOVIA, NY 13035
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
93907	CAMCAR DIV OF TEXTRON INC	ATTN: ALICIA SANFORD 516 18TH AVE	ROCKFORD, IL 611045181
TK1547	MOORE ELECTRONICS INC	19500 SW 90TH CT PO BOX 1030	TUALATIN, OR 97062
72113	ESCO CORPORATION	2141 N W 25TH	PORTLAND, OR 97210

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6-1-1	672-5506-50			1	CIRCUIT BD ASSY:AGP8X INTERPOSER PROBE W/CABLES,TMS809	80009	672-5506-00
-2	214-3796-00			2	HEAT SINK,SEMIC:ALUMINUM,TO-220,VERTICAL ECB MOUNT,TINNED TAB,576802B03900	30161	576802B03900

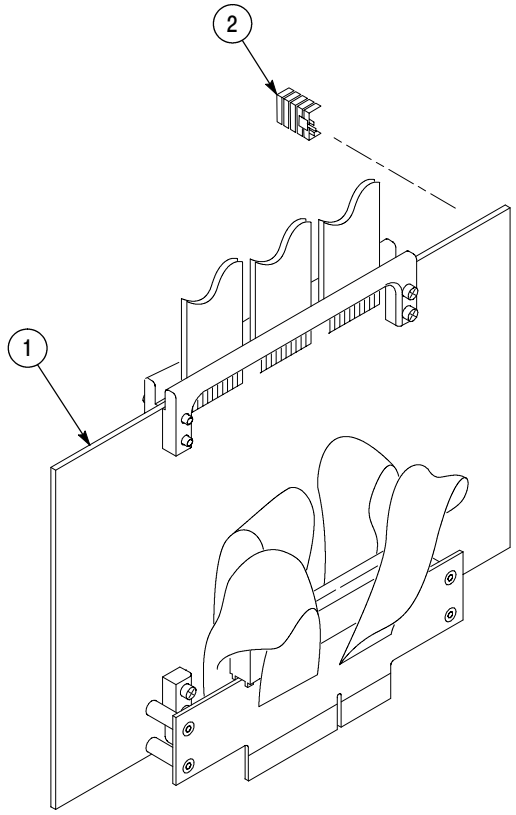

Figure 6-1: Interposer probe head exploded view

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6-2-1	672-5507-50			1	CIRCUIT BD ASSY:AGP8X BACKSIDE PROBE W/CABLE,TMS809	80009	672-5507-50
-2	214-3796-00			2	HEAT SINK,SEMIC:ALUMINUM,TO-220,VERTICAL ECB MOUNT,TINNED TAB,576802B03900	30161	576802B03900
-3	211-0213-00			2	SCREW,MACHINE:4-40 X 0.312,PNH,NYL SLOT	0KB01	ORDER BY DESCRIPTION
-3	210-0975-00			1	WASHER,SHLDR:0.14 ID X 0.375 OD X 0.1 THK,DERLIN	0KB01	210-0975-00
-4	220-0260-00			4	NUT:EXTENSION NUT,DRILL/TAP FOR 2-56 THREAD,301 SSTL	TK0588	220-0260-00
-5	119-6803-00			1	ASSEMBLY,POGO PIN;TMS809	80009	119-6803-00
-6	211-0112-00			1	SCREW,MACHINE:2-56 X 0.375,FLH,100 DEG,STL CD PL,POZ	93907	ORDER BY DESCRIPTION
-7	391-0245-00			2	BLOCK,MOUNTING:FR4,TMS809	5Y400	391-0245-00

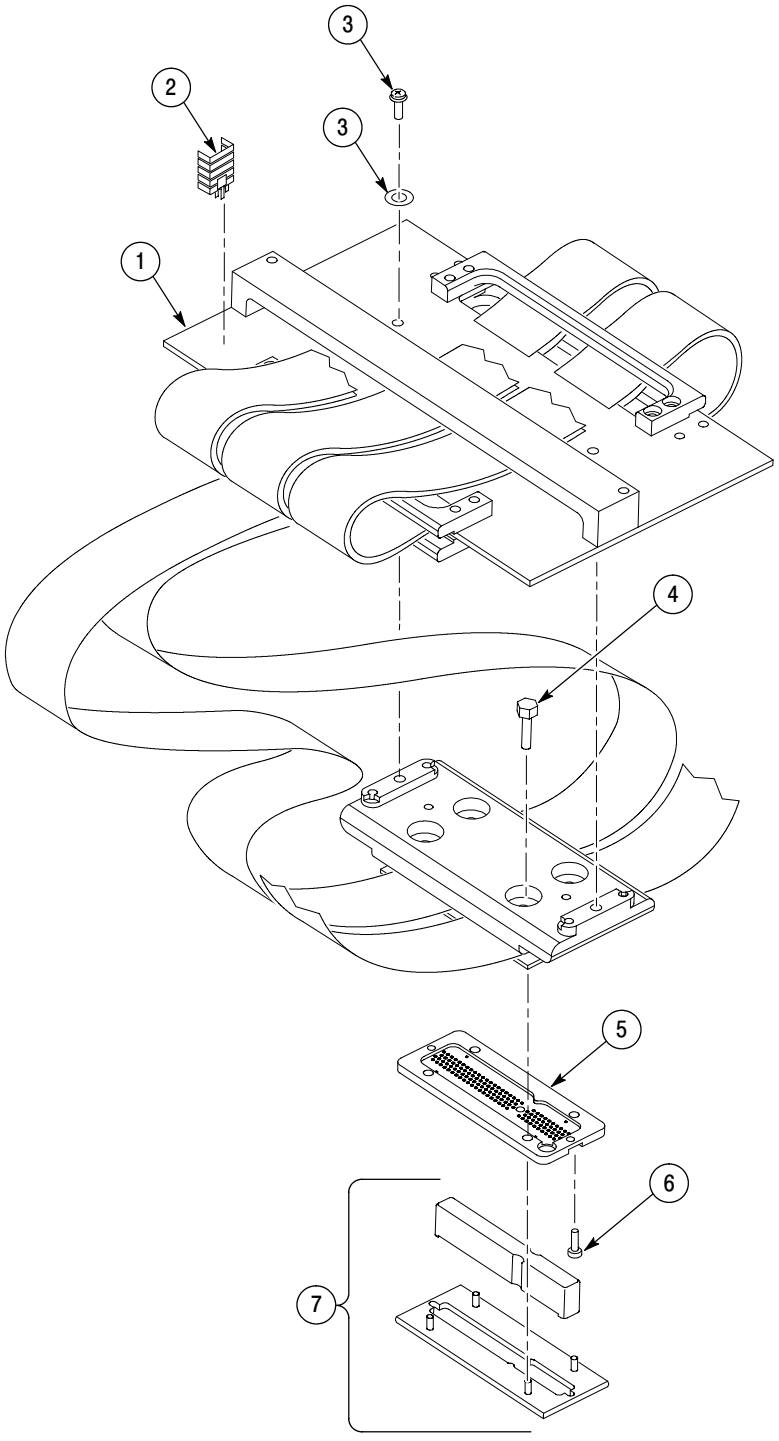

Figure 6-2: Backside probe head exploded view

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6-3-1	671-5505-00			1	CIRCUIT BD ASSY:AGP8X LOGIC, WIRED,TMS809	80009	671-5505-50
-2	174-2699-00			1	CA,ASSY SP:DISCRETE,SLDR/CRIMP,26 AWG,10.0 L,1 X 2,0.1 CTR RCPT X GRN LED	TK1547	174-2699-00
-3	210-0390-00			1	RIVET,SNAP:0.501 LONG,WHEN INSTALLED,BLACK,NYLON,SR-4100B	06915	SR-4100B
-4	119-5832-00			1	FILTER,RFI:LINE FILTER,6A,50/60 HZ,115/260 VAC,LEAKAGE CURRENT 0.4MA AT 250VAC/60HZ,06GENG	0ADN8	06GENG3E
-5	260-1961-00			1	SWITCH,ROCKER:DPST,6(4)A,250V UL APVD	7W718	1802.1121
-6	212-0001-00			1	SCREW,MACHINE:8-32 X 0.25,PNH,STL CD PL,POZ	1AW87	ORDER BY DESCRIPTION
-7	174-4710-00			1	CA ASSY:POWER,DISCRETE,YELLOW,14 AWG,54.0L,INSULATION RATED TO 600V & 105 DEG C,DUAL END,(SET OF THREE CABLES)		174-4710-00
-8	348-0430-00			4	BUMPER,PLASTIC:POLYURETHANE,BLACK	2K262	ORDER BY DESCRIPTION
-9	131-4356-00			1	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,30 GOLD	26742	9618-302-50
-10	262-1036-00			1	SWITCH,ROCKER;SPDT,ON-ON,6A,250V,SILVER CONTACTS,SNAP IN PANEL MOUNT, W/ CABLE AS-SEMBLY;MARQUARDT 1803.1102 SWITCH	72113	1803.1102
-11	119-5637-00			1	POWER SUPPLY:375W,CUSTOM AC-DC,85-264VRMS 47-63HZIN,+5V@40A,5V@3A,+12V10A,12V@6A,ACTIVEPFC	54407	PFC375-4000
-12	211-0538-00			1	SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG,STL CD PL,POZ	93907	ORDER BY DESCRIPTION
-13	119-5935-00			1	FAN,TUBEAXIAL:DC,12V,0.15 A,1.8 W,48CFM,2450 RPM,30 DBA,SLEEVE,92MM X 92MM X 26 MM,10.6 LEAD	61058	FBA09A12M1A
-14	378-0454-00			1	GUARD,FAN:4 POSITION	0D1M6	055013
-15	212-0070-00			1	SCREW,MACHINE:8-32 X 0.312,FLH,100 DEG,STL CD PL,POZ	0KB01	ORDER BY DESCRIPTION
-16	211-1050-00			1	SCREW,MACHINE:6-32 X 0.312 L,PNH,STL CAD PLT,T15	0KB01	OBD
---	159-5022-00			1	FUSE:5.0A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL REG,CSA CERT,451005	75915	R451010
---	159-5015-00			1	FUSE,SMD:10.0A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL REG,CSA CERT	75915	R451010
---	159-0059-00			1	FUSE,WIRE LEAD:5A,125V	61857	SPI-5A
					STANDARD ACCESSORIES		
	071-1084-00			1	MANUAL,TECH:INSTRUCTION,AGP8X SOFTWARE/HARDWARE,TMS809	TK2548	071-1084-00
	161-0104-00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH,RTANG,IEC320,RCPT X STR,NEMA 15-5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION

Replaceable parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	----------*			1	P6434 34CH HIDENSITY PROBE*: FOR TLA7LX/7MX	80009	P6434
	----------*			1	P6860 34 CH PROBE*: FOR TLA7AXX,HIGH DENSITY COMPRESSION,SINGLE ENDED/DIFFERENTIAL CLOCK	80009	P6860
	161-0104-05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,AUSTRALIA,SAFTEY CONTROLLED	TK1373	161-0104-05
	161-0104-06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,EUROPEAN,SAFTEY CONTROLLED	TK1373	ORDER BY DESCRIPTION
	161-0104-07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG,IEC320,RCPT X 13A,FUSED,UK PLUG,(13A FUSE),UK PLUG,(13A FUSE),UNITED KINGDOM,SAFTEY CONTROLLED	TK2541	ORDER BY DESCRIPTION
	161-0167-00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,SWISS,NO CORD GRIP,SAFTEY CONTROLLED	S3109	ORDER BY DESCRIPTION

*** Check the P6434 Probe manual or P6860 Probe manual (Tektronix.com.) for detailed replaceable part number information.**

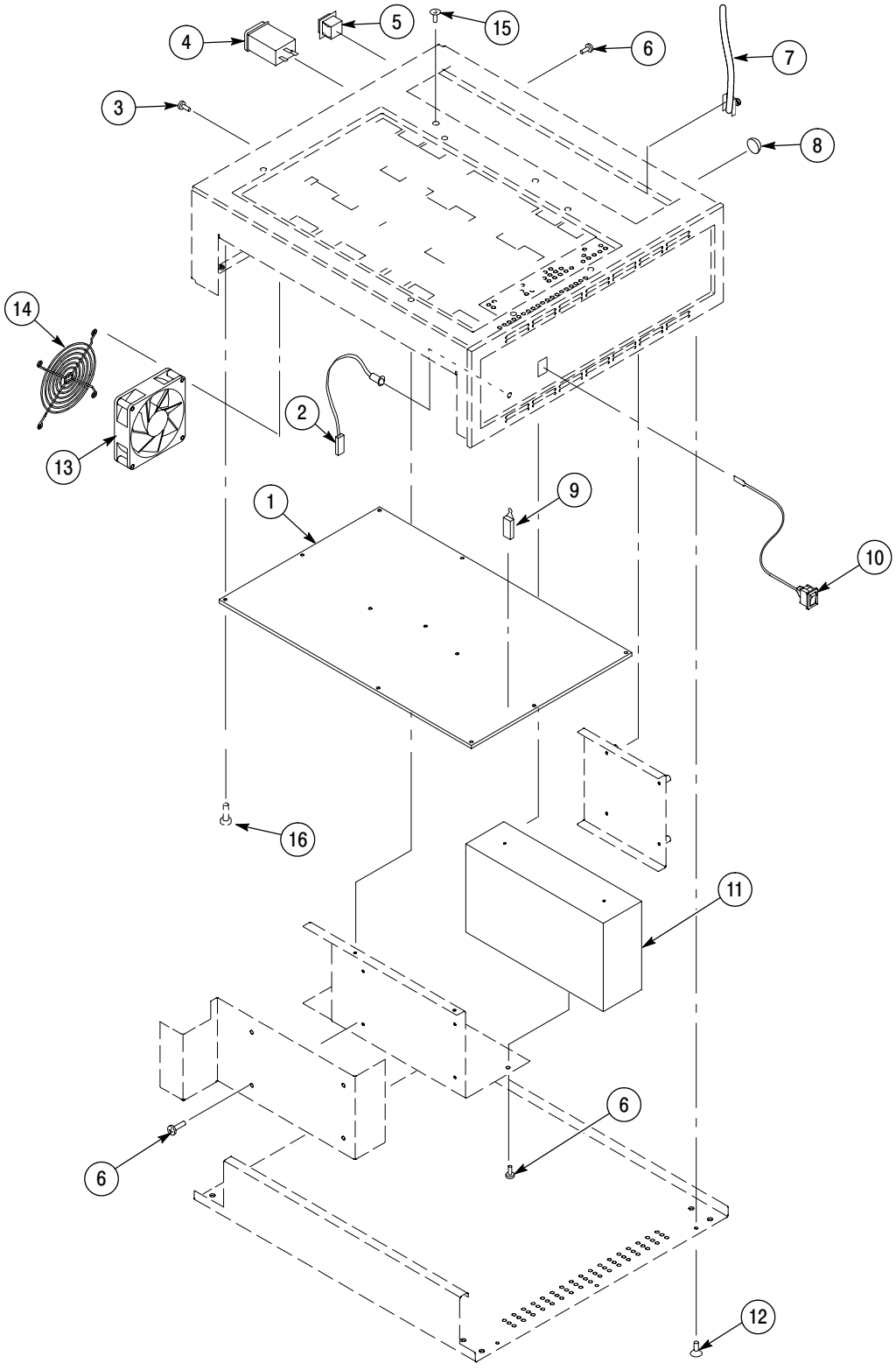

Figure 6-3: Preprocessor unit exploded view

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